A-823

Hardware Manual

Warranty

All products manufactured by ICP DAS are warranted against defective materials for a period of one year from the date of delivery to the original purchaser.

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1. Introduction

1.1 General Description

The A-823PGL/PGH is a high performance, multifunction analog, digital I/O board for the PC AT compatible computer. The A-823PGL provides low gain (0.5,1, 2, 4, 8). The A-823PGH provides high gain (0.5,1,5,10,50,100,500,1000). The A-823PGL/PGH contains a 12-bit ADC with up to 16 single-ended or 8 differential analog inputs. The maximum sample rate of A/D converter is about 100Ksample/sec. There are two 12-bits DAC with voltage outputs, 16 channels of TTL-compatible digital input, 16 channels of TTL-compatible digital output and one 16-bit counter/timer channel for timing input and output.

Using ASC-TI486/33M CPU board of ICP as a target PC based system, the performance of A/D conversion is given below :

- **Polling mode : about 100Ksample/sec (with single-task OS)**
- **Interrupt mode : about 60Ksample/sec (with single-task OS)**
- **DMA mode : about 100Ksample/sec (with single-task OS)**

1.2 Features

- The maximum sample rate of A/D converter is about 100 K sample/sec
- Software selectable input ranges
- PC AT compatible ISA bus
- A/D trigger mode : software trigger , pacer trigger, external trigger
- 16 single-ended or 8 differential analog input signals
- Programmable high gain : 0.5,1,5,10,50,100,500,1000 (A-823PGH)
- Programmable low gain : 0.5,1,2,4,8 (A-823PGL)
- 2 channel unipolar / bipolar 12-bit D/A voltage output
- 16 digital input /16 digital output (TTL compatible)
- Interrupt handling
- Bipolar/unipolar operation
- 1 channel general purpose programmable 16 bits timer/counter

1.3 Specifications

1.3.1 Power Consumption :

- +5V @960 mA maximum, A-823PGL/PGH7
- Operating temperature : -20°C ~ 60°C

1.3.2 Analog Inputs

- Channels : 16 single-ended or 8 differential
- Input range : (software programmable)

  A-823PGL:bipolar : ±10V,±5V, ±2.5V, ±1.25V, ±0.0625V

  unipolar : 0~10V, 0~5V, 0~0.2.5V, 0~1.25.V

  A-823PGH:bipolar : ±10,±5V,±1V, ±0.5V, ±0.1V, ±0.05V, ±0.01V, ± 0.005V

  unipolar : 0-~10V, 0~1V, 0~0.1V, 0~0.01V
- Input current : 250 nA max (125 nA typical) at 25 deg.
- On chip sample and hold
- Over voltage : continuous single channel to **70Vp-p**
- Input impedance : 10^{10} Ω // 6pF

Caution : refer to Sec. 2.9 first

1.3.3 A/D Converter

- Type : successive approximation , Burr Brown ADS 774 or SIPEX-SP774B (equivalent)
- Conversion time : 8 microsec.
- Accuracy : +/- 1 bit
- Resolution : 12 bits

1.3.4 DA Converter

- Channels : 2 independent
- Type : 12 bit multiplying , Analog device AD-7541
- Linearity : +/- 1/2 bit
- Output range : 0~5V , 0~10V or ±5V , ±10Vjumper selected , may be used with other AC or DC reference input Maximum output limit +/- 10V
- Output drive : +/- 5mA
- settling time : 0.6 microseconds to 0.01% for full scale step

1.3.5 Digital I/O

- Output port : 16 bits, TTL compatible
- Input port : 16 bits, TTL compatible

1.3.6 Interrupt Channel

- Level : 3,4,5,6,7,10,11,12,14,15, jumper selectable
- Enable : Via control register

1.3.7 Programmable Timer/Counter

- Type : 82C54 -8 programmable timer/counter
- Counters : The counter1 is a 16 bits pacer timer The counter0 is used as user timer/counter or event trigger function. The counter 2 is used as user timer / counter . The software driver use counter0 to implement a machine independent timer.
- Clock input frequency : DC to 10 MHz
- Pacer output : 61Hz to 1MHz
- Input ,gate : TTL compatible
- Internal Clock : 2M Hz
- Event trigger function

1.3.8 Direct Memory Access Channel (DMA)

- Level : CH1 or CH3, jumper selectable
- Enable : via DMA bit of control register
- Termination : by interrupt on T/C
- Transfer rate : 125K conversions/sec.(DOS Software manual, sec. 4.11)

1.4 Applications

- Signal analysis
- FFT & frequency analysis
- Transient analysis
- Production test
- Process control
- Vibration analysis
- Energy management
- Industrial and lab. measurement and control

1.5 Product Check List

In addition to this manual, the package includes the following items:

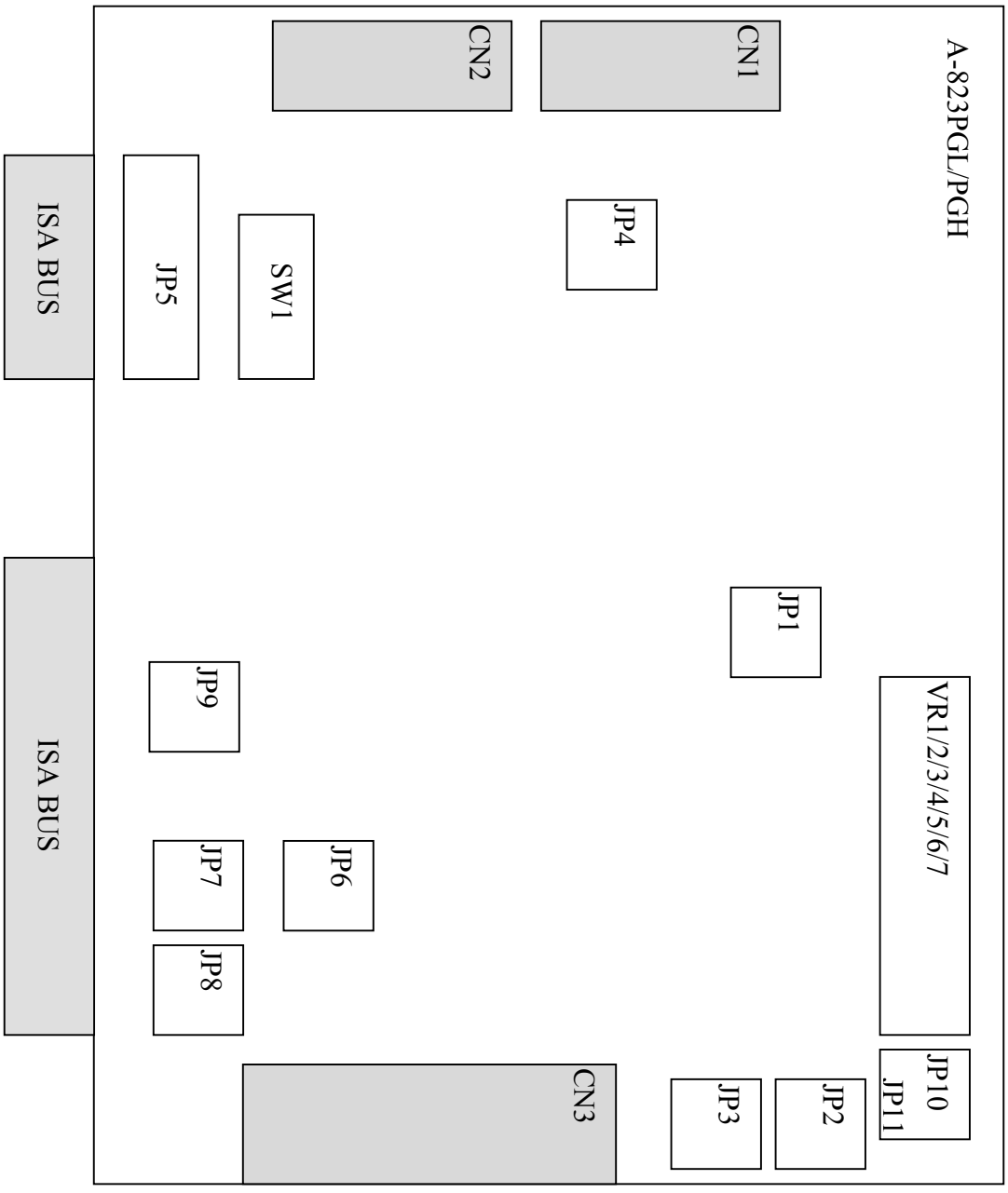
- A-823PGL/PGH multifunction card
- A-823PGL/PGH utility diskette

Attention !

If any of these items is missing or damaged, contact the dealer who provides you this product. Save the shipping materials and carton in case you want to ship or store the product in the future.

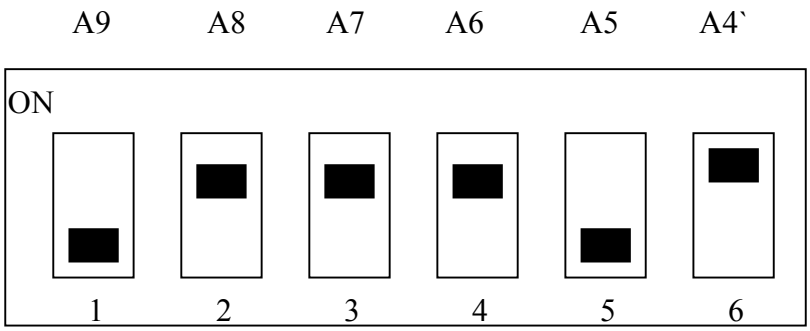
2. Hardware Configuration

2.1 Board Layout



2.2 I/O Base Address Setting

The A-823PGL/PGH occupies 16 consecutive locations in I/O address space.
The base address is set by DIP switch SW1. The default address is 0x220.



SW1 : BASE ADDRESS

BASE ADDR	A9	A8	A7	A6	A5	A4
200-20F	OFF	ON	ON	ON	ON	ON
210-21F	OFF	ON	ON	ON	ON	OFF
220-22F(☑)	OFF	ON	ON	ON	OFF	ON
230-23F	OFF	ON	ON	ON	OFF	OFF
:	:	:	:	:	:	:
300-30F	OFF	OFF	ON	ON	ON	ON
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF

(☑) : default base address is 0x220

The PC I/O port mapping is given below.

ADDRESS	Device	ADDRESS	DEVICE
000-1FF	PC reserved	320-32F	XT Hard Disk
200-20F	Game/control	378-37F	Parallel Printer
210-21F	XT Expansion Unit	380-38F	SDLC
238-23F	Bus Mouse/Alt. Bus Mouse	3A0-3AF	SDLC
278-27F	Parallel Printer	3B0-3BF	MDA/Parallel Printer
2B0-2DF	EGA	3C0-3CF	EGA
2E0-2E7	AT GPIB	3D0-3DF	CGA
2E8-2EF	Serial Port	3E8-3EF	Serial Port
2F8-2FF	Serial Port	3F0-3F7	Floppy Disk
300-31F	Prototype Card	3F8-3FF	Serial Port

2.3 Jumper Setting

Jumper reference table

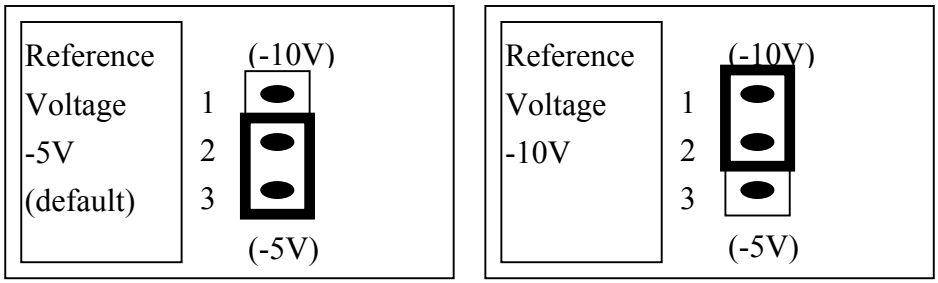
JP1	JP2	JP3	JP4	JP5	JP6
D/A Internal reference voltage selection	D/A Internal/ External reference selection	A/D Single-end/ Differential selection	A/D Internal / External trigger selection	IRQ selection	Internal / External clock selection
Page 10	Page 11	Page 11	Page 12	Page 12	Page 13

JP7	JP8	JP9	JP10	JP11	
DMA DACK channel selection	DMA DRQ channel selection	Event trigger selection	D/A CH0 Unipolar / Bipolar selection	D/A CH1 Unipolar / Bipolar selection	
Page 14	Page 14	Page 13	Page 10	Page 10	

D/A output range jumper setting reference table

JP1	JP2	JP10	JP11	D/A Output range
-5V	Internal	Unipolar	Unipolar	D/A CH0 0~5V D/A CH1 0~5V
-5V	Internal	Bipolar	Unipolar	D/A CH0 ±5V D/A CH1 0~5V
-5V	Internal	Unipolar	Bipolar	D/A CH0 0~5V D/A CH1 ±5V
-5V	Internal	Bipolar	Bipolar	D/A CH0 ±5V D/A CH1 ±5V
-10V	Internal	Unipolar	Unipolar	D/A CH0 0~10V D/A CH1 0~10V
-10V	Internal	Bipolar	Unipolar	D/A CH0 ±10V D/A CH1 0~10V
-10V	Internal	Unipolar	Bipolar	D/A CH0 0~10V D/A CH1 ±10V
-10V	Internal	Bipolar	Bipolar	D/A CH0 ±10V D/A CH1 ±10V

2.3.1 JP1 : D/A Internal Reference Voltage Selection



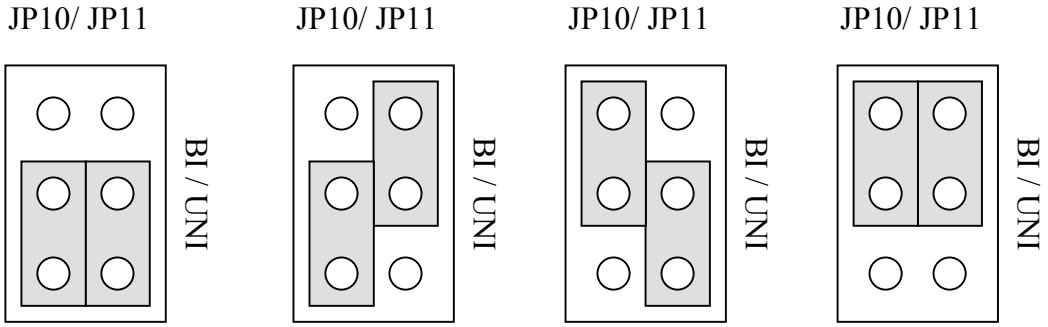
Select (-5V) : D/A voltage output = 0 to 5V (both channel)

Select (-10V) : D/A voltage output = 0 to 10V (both channel)

JP1 is validate only if JP2 select D/A internal reference voltage

2.3.2 JP10 , JP11 D/A Unipolar /Bipolar Operation

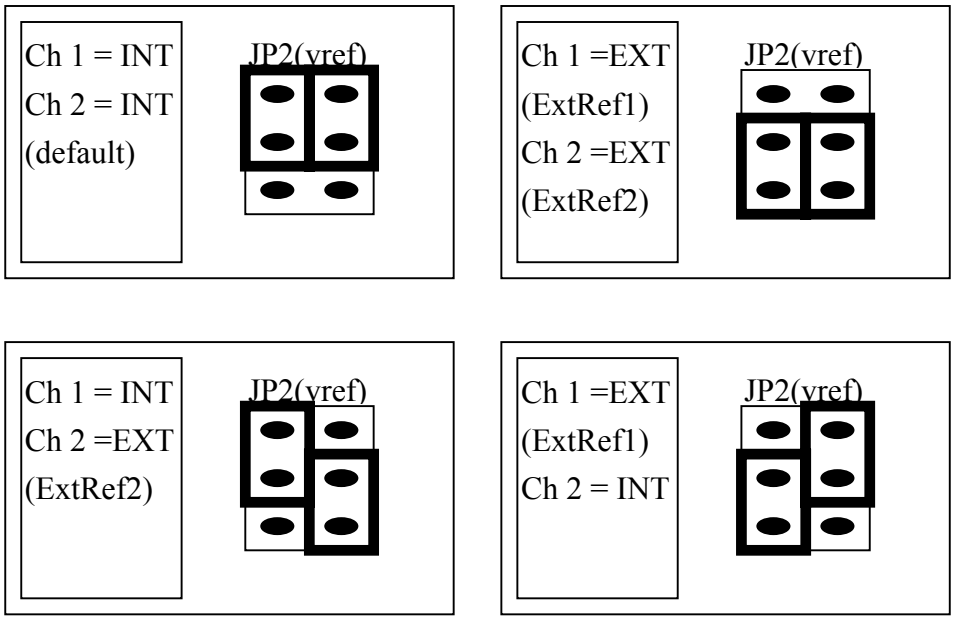
The A-823PG series provides unipolar or bipolar mode analog output , it can be jumper setting by JP10, JP11.The JP10 for D/A channel 10 , JP11 for D/A channel 1



D/A CH 0 unipolar	D/A CH 0 unipolar	D/A CH 0 bipolar	D/A CH 0 bipolar
D/A CH 1 unipolar	D/A CH 1 bipolar	D/A CH 1 unipolar	D/A CH 1 bipolar

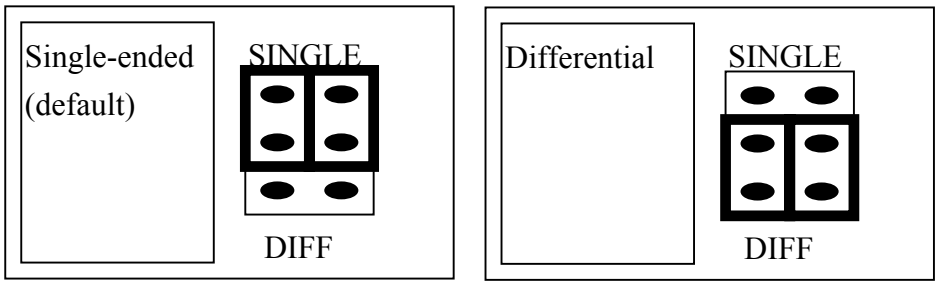
✸Default setting

2.3.3 JP2 : D/A Int/Ext Ref Voltage Selection



If JP2 select **internal reference**, then JP1 select **-5V/-10V** internal reference voltage.
If JP2 select **external reference**, then **ExtRef1, CN3 pin 31**, is the external reference voltage for DA channel 1. and **ExtRef2, CN3 pin 12**, is the external reference voltage for DA Channel 2. If user provides AC +/- 10V external reference voltage, the D/A output voltage may be AC -/+ 10V

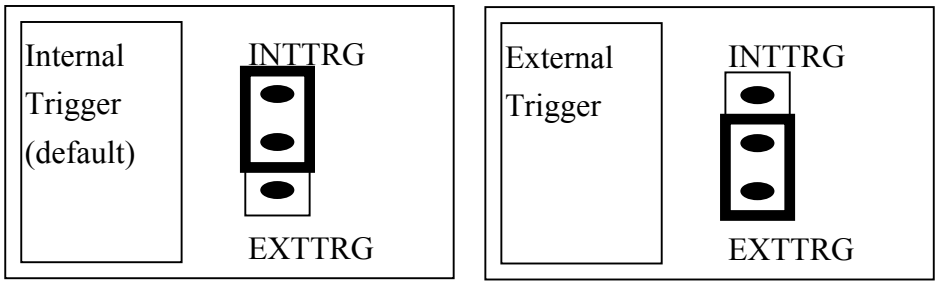
2.3.4 JP3 : Single-ended/Differential Selection



The A-823PGL/PGH offer 16 single-ended or 8 differential analog input signals. The JP3 select single-ended/differential. The user can not select single-ended and differential simultaneously.

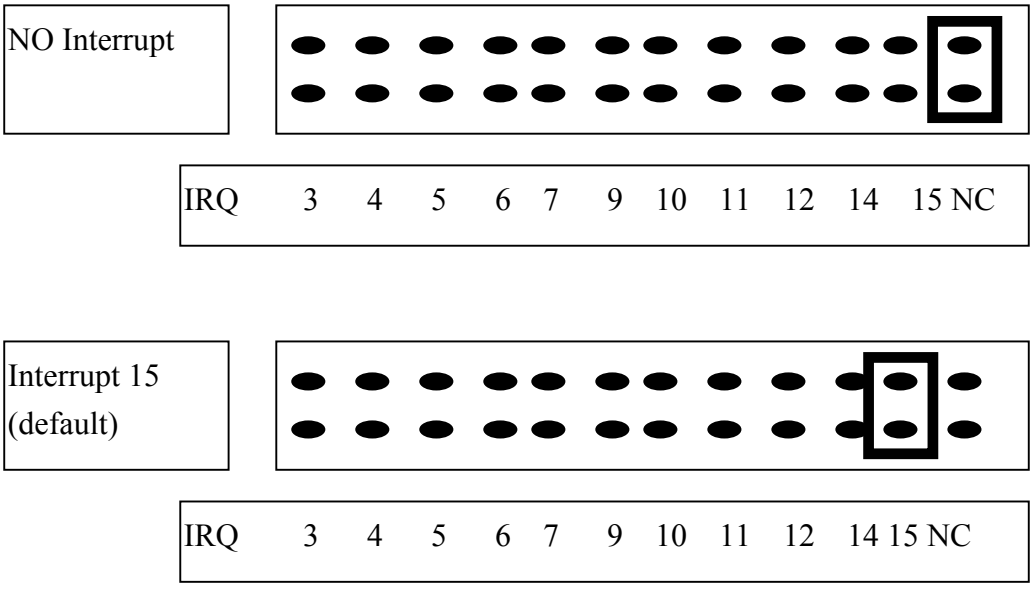
Refer to Sec. 2.9 first.

2.3.5 JP4 : A/D Trigger Source Selection



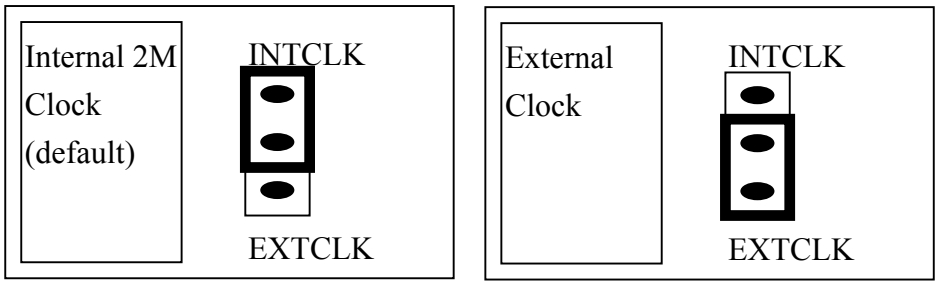
The A-823PGL/PGH supports two trigger type, **internal trigger** and **external trigger.** The external trigger comes from **ExtTrg, CN3 pin 17**. There are two types of internal trigger, **software trigger** and **pacer trigge**r. The details information is given in section 2.4.8.

2.3.6 JP5 : Interrupt Level Selection



The interrupt channel **can not be shared.** The A-823 software driver can support 8 different boards in one system but only **2 of these cards** can use interrupt transfer function.

2.3.7 JP6 : User Timer/Counter Clock Input Selection



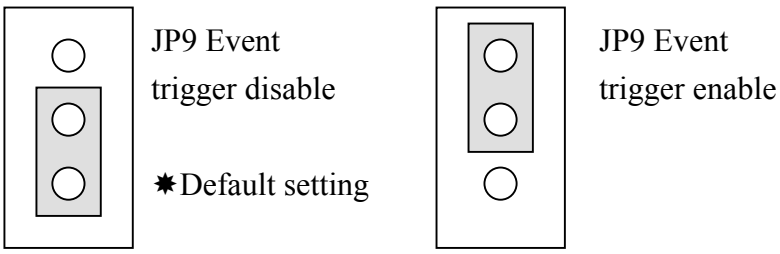
The A-823PGL/PGH has 3 independent 16 bits timer/counter. The cascaded counter1 and counter2 are used as **pacer timer**. The counter0 can be used as a user programmable timer/counter. The user programmable timer/counter can select **2M internal clock** or **external clock ExtCLK, CN3 pin 37**. The block diagram is given in section 2.6. The clock source must be very **stable.** It is recommended to use internal 2M clock.

The 823PGL/PGH software driver use the counter0 as a machine independent timer. If user program call **A-823_Delay()** subroutine, the counter0 will be programmed as a machine independent timer. The detail information is given in section 2.6.

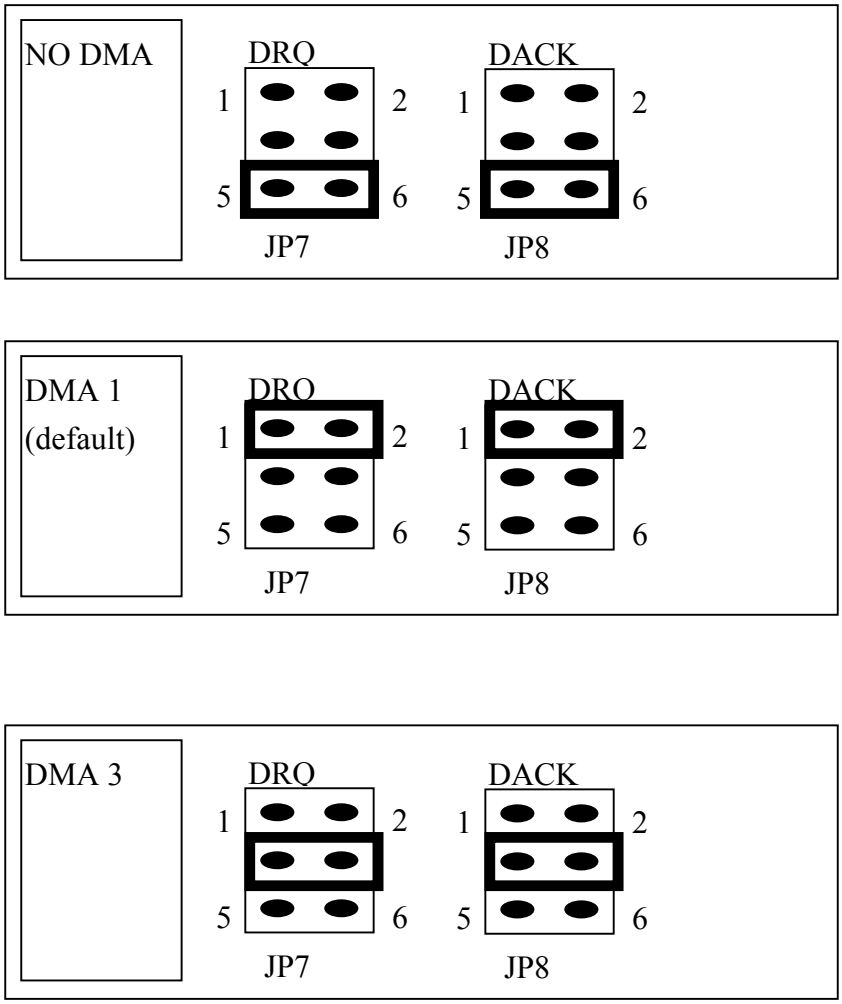
NOTE : if use A-823_Delay(), the JP6 must select internal 2M clock.

2.3.8 JP9 Event Trigger

The A-823PG series provides event trigger function, It can control the 8254 internal trigger gate from the 8254 counter 0 .



2.3.9 JP7 : DMA DACK Selection, JP8 : DMA DRQ Selection



The DMA channel can not shared. The A-823 software driver can support 8 different boards in one PC based system, but only **two of these boards** can use DMA transfer function.

2.4 I/O Register Address

The A-823PGL/PGH occupies 16 consecutive PC I/O addresses. The following table lists the registers and their locations.

Address	Read	Write
Base+0	8254 Counter 0	8254 Counter 0
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control
Base+4	A/D Low Byte	D/A Channel 0 Low Byte
Base+5	A/D High Byte	D/A Channel 0 High Byte
Base+6	DI Low Byte	D/A Channel 1 Low Byte
Base+7	DI High Byte	D/A Channel 1 High Byte
Base+8	Reserved	A/D Clear Interrupt Request
Base+9	Reserved	A/D Gain Control
Base+A	Reserved	A/D Multiplexer Control
Base+B	Reserved	A/D Mode Control
Base+C	Reserved	A/D Software Trigger Control
Base+D	Reserved	DO Low Byte
Base+E	Reserved	DO High Byte
Base+F	Reserved	Reserved

2.4.1 8254 Counter

The 8254 Programmable timer/counter has 4 registers from Base+0 through Base+3. For detailed programming information about 8254 , please refer to Intel‘s “Microsystem Components Handbook”.

Address	**Read**	**Write**
Base+0	8254 Counter 0	8254 Counter 0
Base+1	8254 Counter 1	8254 Counter 1
Base+2	8254 Counter 2	8254 Counter 2
Base+3	Reserved	8254 Counter Control

2.4.2 A/D Input Buffer Register

(READ) Base+4 : A/D Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+5 : A/D High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	READY	D11	D10	D9	D8

A/D 12 bits data : D11…..D0, D11=MSB, D0=LSB
READY =1 : A/D 12 bits data not ready
=0 : A/D 12 bits data is ready

The low 8 bits A/D data are stored in address BASE+4 and the high 4 bits data are stored in address BASE+5. The READY bit is used as a indicator for A/D conversion. **When a A/D conversion is completed, the READY bit will be clear to zero.**

2.4.3 D/A Output Latch Register

(WRITE) Base+4 : Channel 1 D/A Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+5 :Channel 1 D/A High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D11	D10	D9	D8

(WRITE) Base+6 : Channel 2 D/A Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+7 :Channel 2 D/A High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D11	D10	D9	D8

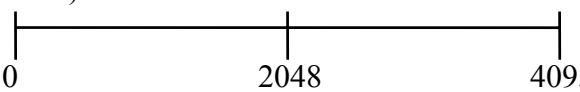
D/A 12 bits output data : D11..D0, D11=MSB, D0=LSB, X=don‘t care

The D/A converter will convert the 12 bits digital data to analog output. The low 8 bits of **D/A channel 1** are stored in address BASE+4 and high 4 bits are stored in address BASE+5. The address BASE+6 and BASE+7 store the 12 bits data for **D/A channel 2**. The D/A output latch registers are designed as a **“double buffered”** structure, so the analog output latch registers will be updated until the high 4 bits digital data are written. If the user send the high 4 bits data first, the DA 12 bits output latch registers will update at once. So the low 8 bits will be the previous data latched in register. **This action will cause an error on DA output voltage**. **So the user must send low 8 bits first and then send high 4 bits to update the 12 bits AD output** latch register.

NOTE : Send low 8 bits first, then send high 4 bits.

D/A data = LSB(D0~D7)+MSB(D8~D11)*256

D/A data format



Reference voltage

Unipolar(-5V/-10V)	0V / 0V	2.5V / 5V	5V / 10V
Bipolar (-5V/-10V)	-5V / -10V	0V / 0V	+5V / +10V

2.4.4 D/I Input Buffer Register

(READ) Base+6 : D/I Input Buffer Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(READ) Base+7 : D/I Input Buffer High Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

D/I 16 bits input data : D15..D0, D15=MSB, D0=LSB

The A-823PGL/PGH provides 16 TTL compatible digital input. The low 8 bits are stored in address BASE+6. The high 8 bits are stored in address BASE+7.

2.4.5 Clear Interrupt Request

(WRITE) Base+8 : Clear Interrupt Request Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don‘t care, XXXXXXXX=any 8 bits data is validate

If A-823PGL/PGH is working in the interrupt transfer mode, a on-board hardware status bit will be set after each A/D conversion. This bit must be **clear by software** before next hardware interrupt. Writing any value to address BASE+8 will clear this hardware bit and the hardware will generate another interrupt when next A/D conversion is completed.

2.4.6 A/D Gain Control Register

(WRITE) Base+9 : A/D Gain Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	GAIN3	GAIN2	GAIN1	GAIN0

The Only difference between A-823PGL and A-823PGH is the **GAIN** control function. The **A-823PGL provides gain factor of 1/2/4/8** and **A-823PGH provides 1/10/100/1000.** The gain control register control the gain of A/D input signal. Bipolar/Unipolar will effect the gain factor.
It is important to select the correct gain-control-code according to Bipolar/Unipolar input.

NOTE : If gain control code changed, the hardware need to delay extra gain settling time. The gain settling time is different for different gain control code. **The software driver does not take care the gain settling time, so the user need to delay the gain settling time if gain changed.** If the application program need to run in different machines, the user need to implement a machine independent timer. The software driver, **A-823_delay(),** is designed for this purpose. If user use this subroutine then the counter2 introduced in sec 2.6 is reserved by software driver to implement this machine independent timer.

A-823PGL GAIN CONTROL CODE TABLE

BI/UNI	Settling Time	GAIN	Input Range	GAIN3	GAIN2	GAIN1	GAIN0
BI	23 us	1	+/- 5V	0	0	0	0
BI	23 us	2	+/- 2.5V	0	0	0	1
BI	25 us	4	+/- 1.25V	0	0	1	0
BI	28 us	8	+/- 0.0625V	0	0	1	1
UNI	23 us	1	0V ~ 10V	0	1	0	0
UNI	23 us	2	0V ~ 5V	0	1	0	1
UNI	25 us	4	0V ~ 2.5V	0	1	1	0
UNI	28 us	8	0V ~ 1.25V	0	1	1	1
BI	23 us	0.5	+/- 10V	1	0	0	0

BI=Bipolar, UNI=Unipolar, X=don‘t care, N/A=not available

A-823PGH GAIN CONTROL CODE TABLE

BI/UN	Settling Time	GAIN	Input Range	GAIN3	GAIN2	GAIN1	GAIN0
BI	23 us	1	+/- 5V	0	0	0	0
BI	28 us	10	+/- 0.5V	0	0	0	1
BI	140 us	100	+/- 0.05V	0	0	1	0
BI	1300 us	1000	+/- 0.005V	0	0	1	1
UNI	23 us	1	0 ~ 10V	0	1	0	0
UNI	28 us	10	0 ~ 1V	0	1	0	1
UNI	140 us	100	0 ~ 0.1V	0	1	1	0
UNI	1300 us	1000	0 ~ 0.01V	0	1	1	1
BI	23 us	0.5	+/- 10V	1	0	0	0
BI	28 us	5	+/- 1V	1	0	0	1
BI	140 us	50	+/- 0.1V	1	0	1	0
BI	1300 us	500	+/- 0.01V	1	0	1	1

BI=Bipolar, UNI=Unipolar, X=don‘t care, N/A=not available

2.4.7 A/D Multiplex Control Register

(WRITE) Base+A : A/D Multilexer Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	D3	D2	D1	D0

A/D input channel selection data = 4 bits : D3..D0, D3=MSB, D0=LSB, X=don‘t care

Single-ended mode : D3..D0

Differential mode : D2..D0, D3=don’t care

The A-823PGL/PGH provides 16 single-ended or 8 differential analog input signals. In single-ended mode D3..D0 select the active channel. In differential mode D2..D0 select the active channel and D3 will be don’t care.

NOTE: The settling time of multiplexer depend on source resistance.of input sources.

source resistance = about 0.1K ohm → settling time = about 3 us.

source resistance = about 1K ohm → settling time = about 5 us.

source resistance = about 10K ohm → settling time = about 10 us.

source resistance = about 100K ohm → settling time = about 100 us.

Sec 2.4.6 gives information about how to delay the settling time.

2.4.8 A/D Mode Control Register

(WRITE) Base+B : A/D Mode Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	D2	D1	D0

X=don‘t care

JP4 Select Internal Trigger							
Mode Select			Trigger Type		Transfer Type		
D2	D1	D0	Software Trig	Pacer Trig	Software	Interrupt	DMA
0	0	0	X	X	X	X	X
0	0	1	Select	X	Select	X	X
0	1	0	X	Select	X	X	Select
1	1	0	X	Select	Select	Select	X

X=disable

JP4 Select External Trigger						
Mode Select			Trigger Type	Transfer Type		
D2	D1	D0	External Trigger	Software	Interrupt	DMA
0	0	0	X	X	X	X
0	0	1	X	X	X	X
0	1	0	Select	X	X	Select
1	1	0	Select	Select	Select	X

The A/D conversion operation can be divided into 2 stage, **trigger stage and transfer stage**. The trigger stage will generate a trigger signal to A/D converter and the transfer stage will transfer the result to the CPU.

The trigger method may be **internal trigger** or **external trigger.** The internal trigger can be **software trigger** or **pacer trigger. The software trigger is very simple but can not control the sampling rate very precisely.** In software trigger mode, the program issues a software trigger command (sec 2.4.9) any time needed. Then the program will poll the A/D status bit until the ready bit is 0(sec 2.4.2).

The pacer trigger can control the sampling rate very precisely. So the converted data can be used to reconstructed the waveform of analog input signal. In pacer trigger mode, the pacer timer (sec 2.6) will generate trigger signals to A/D converter periodic. These converted data can be transfer to the CPU by polling or interrupt or DMA transfer method.

The software driver provides three data transfer methods, **polling, interrupt and DMA.** The polling subroutine, A-823_AD_PollingVar() or A-823_AD_PollingArray(), set A/D mode control register to **0x01.** This control word means software trigger and polling transfer. The interrupt subroutine, A-823_AD_INT_START(…), set A/D mode control mode register to **ox06.** This control word means pacer trigger and interrupt transfer. The DMA subroutine, A-823_AD_DMA_START(…), set A/D mode control register to **0x02**. This control word means pacer trigger and DMA transfer.

Please refer to sec. 2.7 for detail information.

2.4.9 A/D Software Trigger Control Register

(WRITE) Base+C : A/D Software Trigger Control Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	X	X	X

X=don‘t care, XXXXXXXX=any 8 bits data is validate

The A/D converter can be triggered by software trigger or pacer trigger. The details information is given in sec. 2.4.8 and sec. 2.7. Writing any value to address BASE+C will generate a trigger pulse to A/D converter and initiated a A/D conversion operation. The address BASE+5 offers a ready bit to indicate a A/D conversion complete.

The software driver use this control word to detect the A-823PGL/PGH hardware board. **The software initiates a software trigger and check the ready bit** . If the ready bit can not clear to zero in a fixed time, the software driver will return a error message. If the I/O BASE address setting error, the ready bit will not be clear to zero. The software driver, **A-823_CheckAddress()**, use this method to detect the correctness of I/O BASE address setting

2.4.10 D/O Output Latch Register

(WRITE) Base+D : D/O Output Latch Low Byte Data Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0

(WRITE) Base+E : D/O Output Latch High Byte Data Format

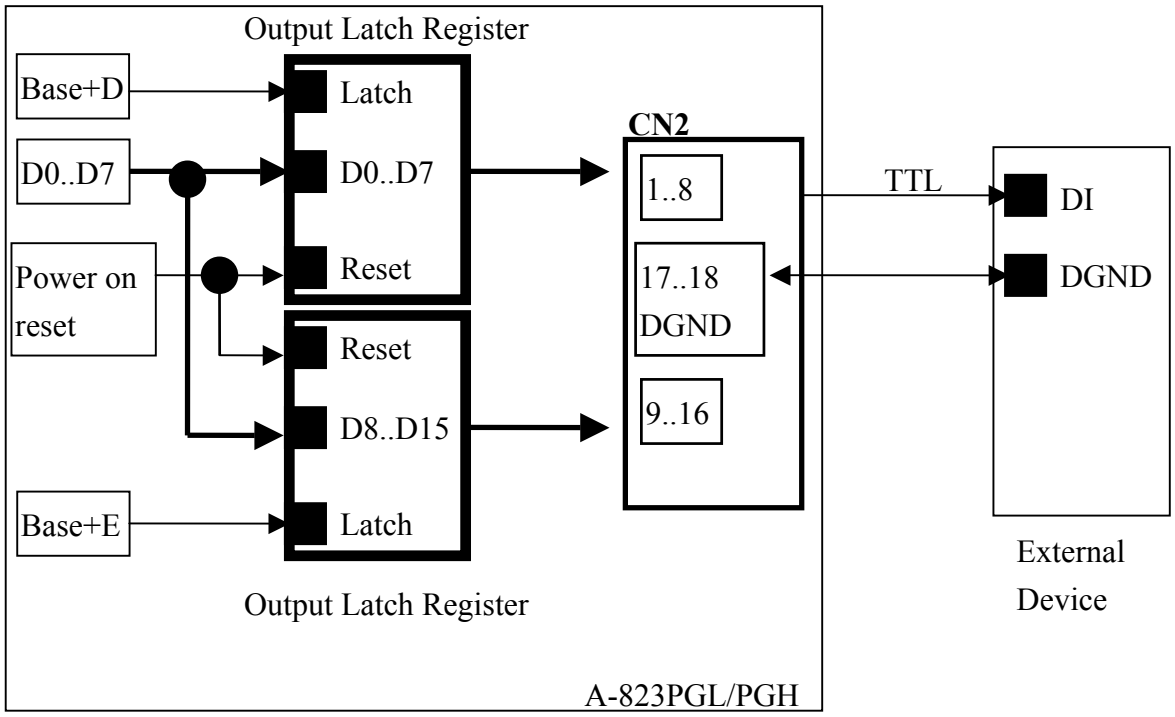
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8

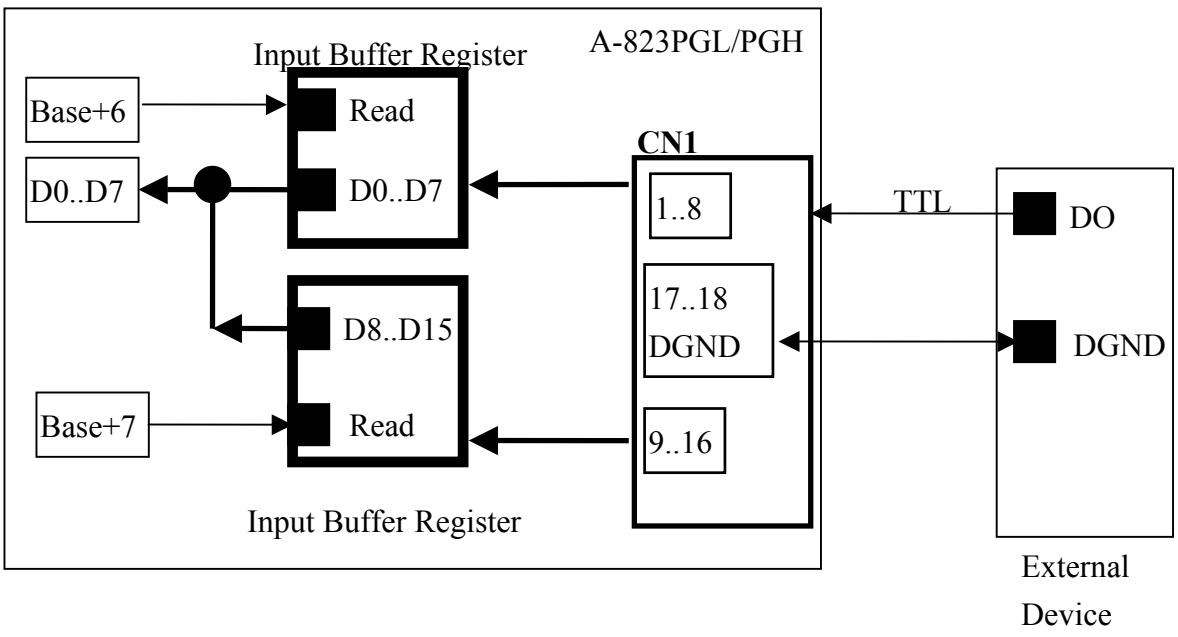
D/O 16 bits output data : D15..D0, D15=MSB, D0=LSB

The A-823PGL/PGH provide 16 TTL compatible digital output. The low 8 bits are stored in address **BASE+D.** The high 8 bits are stored in address **BASE+E**

2.5 Digital I/O

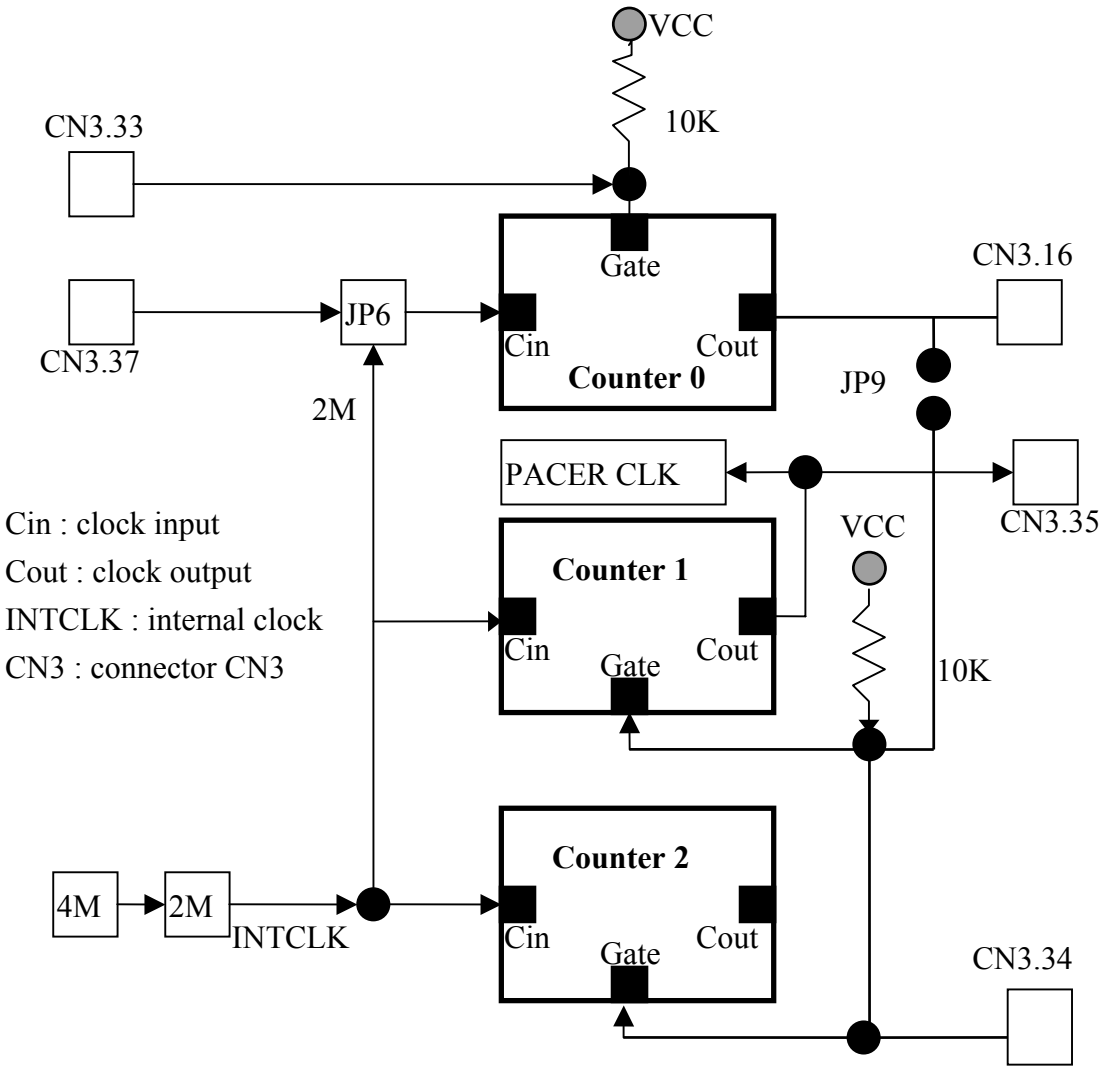
The A-823PGL/PGH provides 16 digital input channels and 16 digital output channels. All levels are TTL compatible. The connections diagram and block diagram are given below:





2.6 8254 Timer/Counter

The 8254 Programmable timer/counter has 4 resgisters from Base+0 through Base+3. For detailed programming information about 8254 , please refer to Intel‘s “Microsystem Components Handbook”.The block diagram is as below.



The counter0, counter1 and counter2 are all 16 bits counter. The COUT of counter 0 can control counter 1 gate by JP9 setting. The counter1 is 16 bits timer is used as **pacer timer**. **The software driver, A-823_Delay(), use counter 0 to implement a machine independent timer for settling time delay (sec. 2.4.6 and sec. 2.4.7).** If user doesn’t use A-823_Delay(), the counter0 can be used as a general purpose timer/counter.

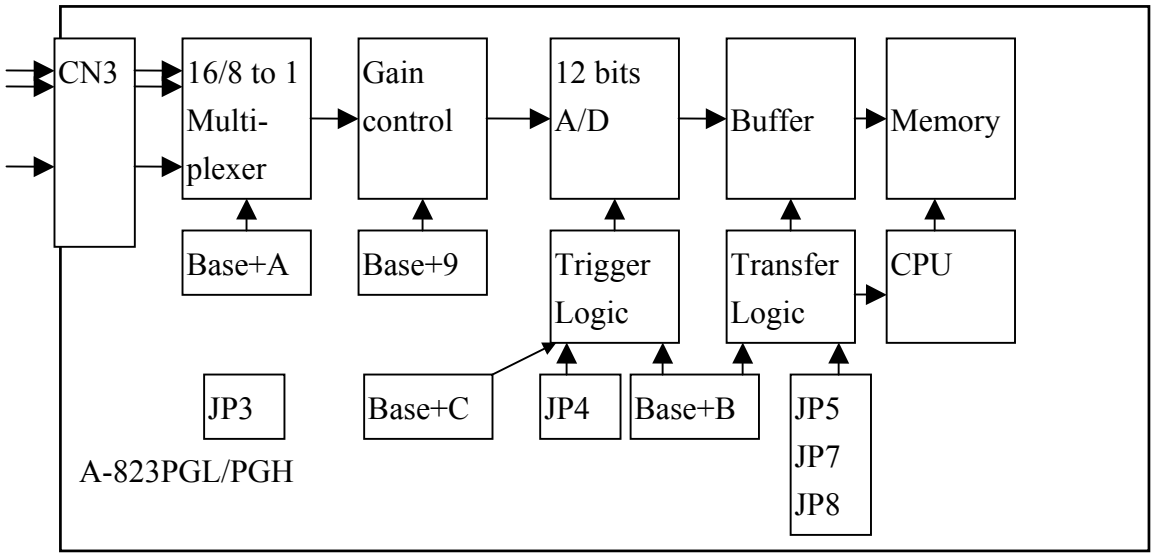
NOTE : When user call A-823_Delay() to implement a machine independent timer, the JP6 must select internal 2M clock.

2.7 A/D Conversion

This section explains how to use A/D conversions. The A/D conversion can be triggered in any of 3 ways, **by software trigger, by pacer trigger or by external trigger** to the A/D converter. At the end of A/D conversion, it is possible to transfer data by any of 3 ways, those are **polling , interrupt and DMA.** Before use the A/D conversion function, user should notice the following issue:

- A/D data register, BASE+4/BASE+5, store the A/D conversion data **(sec. 2.4.2)**
- A/D gain control register, BASE+9, select gain **(sec. 2.4.6)**
- A/D multiplex control register, BASE+A, select analog input **(sec. 2.4.7)**
- A/D mode control register, BASE+B, select trigger type and transfer type **(sec. 2.4.8)**
- A/D software trigger control register, BASE+C **(sec. 2.4.9)**
- JP3 select single-ended or differential input **(sec. 2.3.3)**
- JP4 select internal/external trigger **(sec. 2.3.4)**
- JP5 select IRQ level **(sec. 2.3.5)**
- JP6 select internal/external clock for counter0 **(sec. 2.3.6)**
- JP7,JP8 select DMA channel **(sec. 2.3.7)**
- **3 trigger logic : software, pacer, external trigger (sec. 2.4.8)**
- **3 transfer logic : polling, interrupt, DMA (sec. 2.4.8)**

The block diagram is given below:



2.7.1 A/D conversion flow

Before using the A/D converter, the user should setup the following hardware item :

1. select single-ended or differential input (JP3) **(refer to Sec. 2.9 first)**
2. select internal trigger or external trigger (JP4)
3. select IRQ level if needed (JP5)
4. select DMA channel if needed (JP7,JP8)
5. select internal clock or external clock for counter0 if needed (JP6)

Then the user must decide which A/D conversion mode will be used. The software driver supports three different modes: **polling, interrupt and DMA.** The user can control the A/D conversion by polling mode very easy (sec. 2.4.9). It is recommended to use the software driver if using interrupt or DMA mode.

The analog input signals come from CN3. These signals may be single-ended or differential type and must match with the setting of JP3.

The multiplexer can select 16 single-ended or 8 differential signals into the gain control module. T**he settling time of multiplexer depends on the source resistance.** Because the software **don't take care the settling time**, **the user should delay enough settling time if switching from one channel to next channel. (sec. 2.4.7)**

The gain control module also need settling time if gain control code changed. Because the software **don't take care the settling time**, **the user should delay enough settling time if gain control code ischanged. (sec. 2.4.6)**

The software driver provides **a machine independent timer , A-823_Delay()**, for settling time delay. This subroutine assume that JP6 select internal 2M clock and use counter0 to implement a machine independent timer. If the user call A-823_delay(), the counter0 will be reserved and can't be used as a user programmable timer/counter.

The output of gain control module feed into the A/D converter. **The A/D converter need a trigger signal to start a A/D conversion cycle**. The A-823PGL/PGH supports three trigger mode, **software, pacer and external trigger**. The result of A/D conversion can be transfer into CPU by three mode : **polling, interrupt and DMA**. The operation mode is introduced in **sec. 2.4.8.**

2.7.2 A/D Conversion Trigger Modes

A-823PGL/PGH supports three trigger modes.

1 : Software Trigger :

Write any value to A/D software trigger control register, BASE+A, will initiate a A/D conversion cycle. This mode is very simple but very difficult to control sampling rate.

2 : Pacer Trigger Mode :

The block diagram of pacer timer is show in section 2.6. The pacer timer can give very precise sampling rate.

3 : Enevt Trigger Mode :

The block diagram of event trigger timer is show in section 2.6 . The jumper setting & programming same as the pacer trigger mode only JP9 set to event trigger enable . this function is use external signal via counter 0 to control counter 1 gate then the internal pacer trigger signal will be enable or disable by external signal control.

4 : External Trigger Mode :

When a rising edge of external trigger signal is applied, a A/D conversion will be performed. The external trigger source comes from pin 17 of CN3.

2.7.3 A/D Transfer Modes

A-823PGL/PGH supports three transfer modes.

1 : polling transfer :

This mode can be used with all trigger mode. The detail information is given in section 2.4.8. The software scans A/D high byte data register, BASE+5, until READY_BIT=0.The low byte data is also ready in BASE+4.

2 : interrupt transfer :

This mode can be used with pacer trigger or external trigger. The detail information is given in section 2.4.8.The user can set the IRQ level by adjusting JP5. A hardware interrupt signal is sent to the PC when a A/D conversion is completed.

3 : DMA transfer :

This mode can be used with pacer trigger or external trigger. The detail information is given in section 2.4.8. The user can set the DMA channel by adjusting JP7,JP8. Two hardware DMA requests signal are sent sequentially to the PC when a A/D conversion is completed. The single mode transfer of 8237 is suggested.

If using interrupt or DMA transfer, it is recommended to use A-823 software driver.

2.7.4 Using software trigger and polling transfer

If the user need to direct control the A/D converter without the A-823 software driver. It is recommended to use software trigger and polling transfer. The program steps are listing as below:

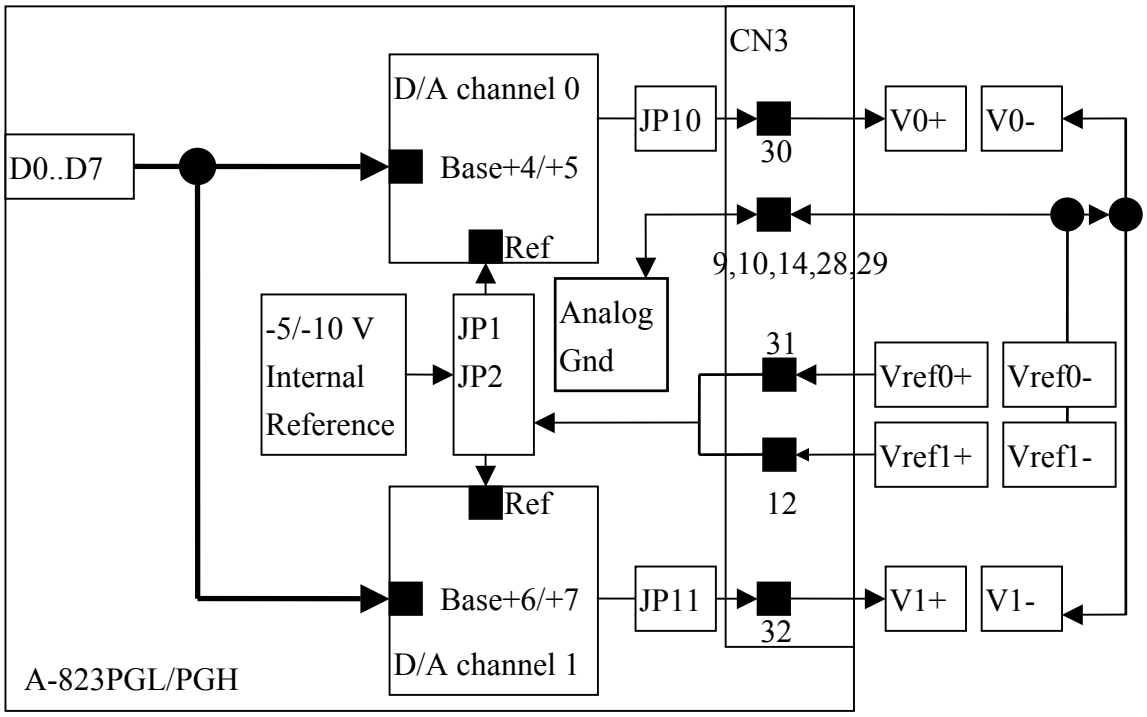
1. send 0x01 to A/D mode control register (software trigger + polling transfer) **(refer to Sec. 2.4.8)**
2. send channel number to multiplexer control register **(refer to Sec.** 2.4.7)
3. send the gain control code value to gain control register **(refer to Sec 2.4.6)**
4. delay the settling time **(refer to Sec. 2.4.6 and Sec. 2.4.7)**
5. send any value to software trigger control register to generate a software rigger signal **(refer to Sec. 2.4.9)**
6. scan the READY bit of the A/D high byte data until READY=0 **(refer to Sec. 2.4.2)**
7. read the 12 bits A/D data **(refer to Sec. 2.4.2)**
8. convert this 12 bits binary data to the floating point value

2.8 D/A Conversion

The A-823PGL/PGH provides two 12 bits D/A converters. Before using the D/A conversion function, user should notice the following issue:

- D/A output register, BASE+4/BASE+5/BASE+6/BASE+7, (sec. 2.4.3)
- JP1 select internal reference voltage -5V/-10V (sec. 2.3.1)
- JP2 select internal/external reference voltage (sec. 2.3.3)
- JP3 select unipolar/bipolar operation mode (sec. 2.3.2
- If JP2 select internal and JP1 select -5V and JP10 select unipolar , the D/A output range from 0 to 5V.
- If JP2 select internal and JP1 select -10V and JP11 select unipolar , the D/A output range from 0 to 10V.
- If JP2 select internal and JP1 select -5V and JP10 select bipolar , the D/A output range from -5V to +5V.
- If JP2 select internal and JP1 select -10V and JP11 select bipolar , the D/A output range from -10V to +10V.
- If JP2 select external, the external reference voltage can be AC/DC +/- 10V

The block diagram is given as below:



NOTE : The DA output latch registers are designed as “double buffer” structure. **The user must send the low byte data first, then send the high byte data to store the DA 12 bits digital data**. If the user only send the high byte data , then the low byte data will be still the previous value. Also if the user send high byte first then send low byte, the low byte data of DA are still hold in the previous one.

D/A output range jumper setting reference table

JP1	JP2	JP10	JP11	D/A Output range
-5V	Internal	Unipolar	Unipolar	D/A CH0 0~5V D/A CH1 0~5V
-5V	Internal	Bipolar	Unipolar	D/A CH0 ±5V D/A CH1 0~5V
-5V	Internal	Unipolar	Bipolar	D/A CH0 0~5V D/A CH1 ±5V
-5V	Internal	Bipolar	Bipolar	D/A CH0 ±5V D/A CH1 ±5V
-10V	Internal	Unipolar	Unipolar	D/A CH0 0~10V D/A CH1 0~10V
-10V	Internal	Bipolar	Unipolar	D/A CH0 ±10V D/A CH1 0~10V
-10V	Internal	Unipolar	Bipolar	D/A CH0 0~10V D/A CH1 ±10V
-10V	Internal	Bipolar	Bipolar	D/A CH0 ±10V D/A CH1 ±10V

2.9 Analog Input Signal Connection

The A-823PGL/PGH can measure single-ended or differential type analog input signal. Some analog signal can be measured in both of single-end or differential mode but some only can be measured in one of the single-ended or differential mode. The user must decide which mode is suitable for measurement.

In general, there are 3 different analog signal connection method as shown in Fig1 to Fig3. The Fig1 is suitable for grounding source analog input signals. The Fig2 can measure more channels than in the Fig1 but only suitable for large analog input signals. The Fig3 is suitable for thermocouple and the Fig4 is suitable for floating source analog input signals. **Note : In Fig3, the maximum common mode voltage between the analog input source and the AGND is 70Vp-p, so the user must make sure that the input signal is under specification first. If the common mode voltage is over 70Vp-p, the input multiplexer will be damaged forever.**

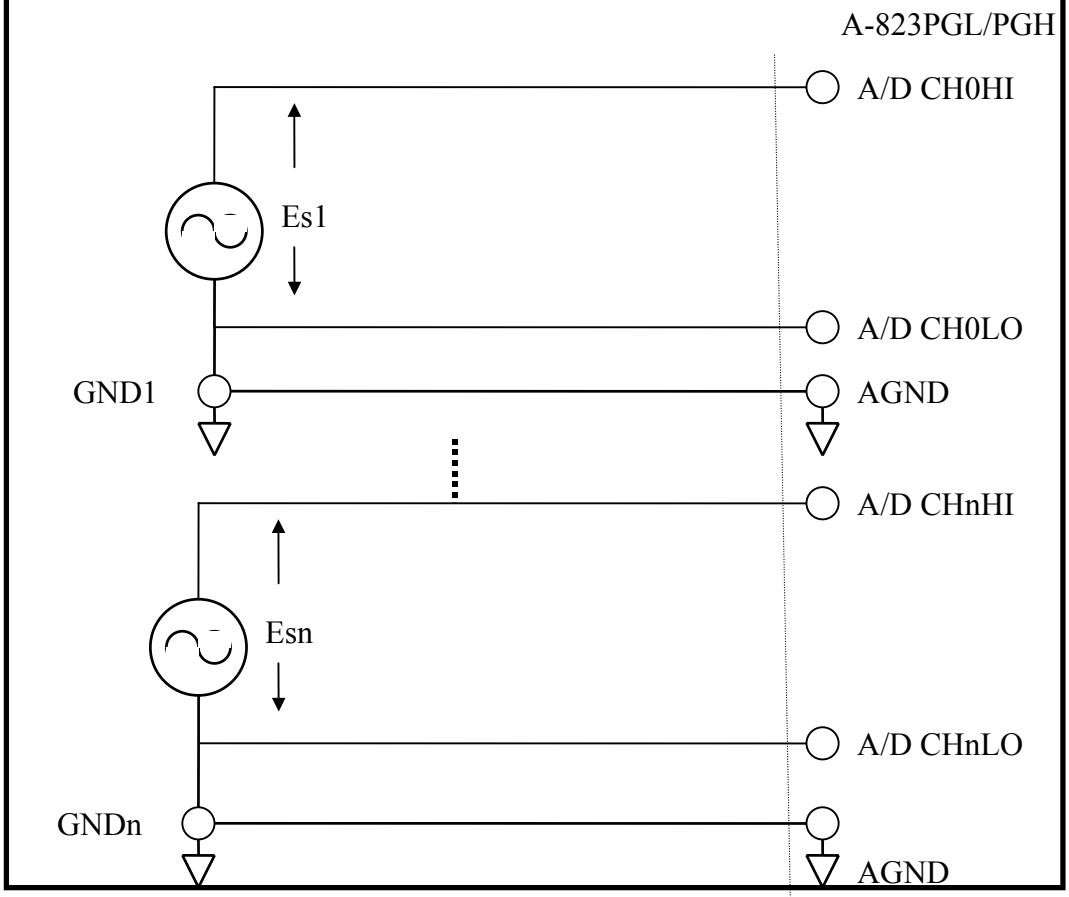
The simple way to select the input signal connection configuration is as below.

1. **Grounding source input signal → select Fig1**
2. **Thermocouple input signal → select Fig3**
3. **Floating source input signal → select Fig4**
4. **If Vin > 0.1V and gain<=10 and need more channels → select Fig2**

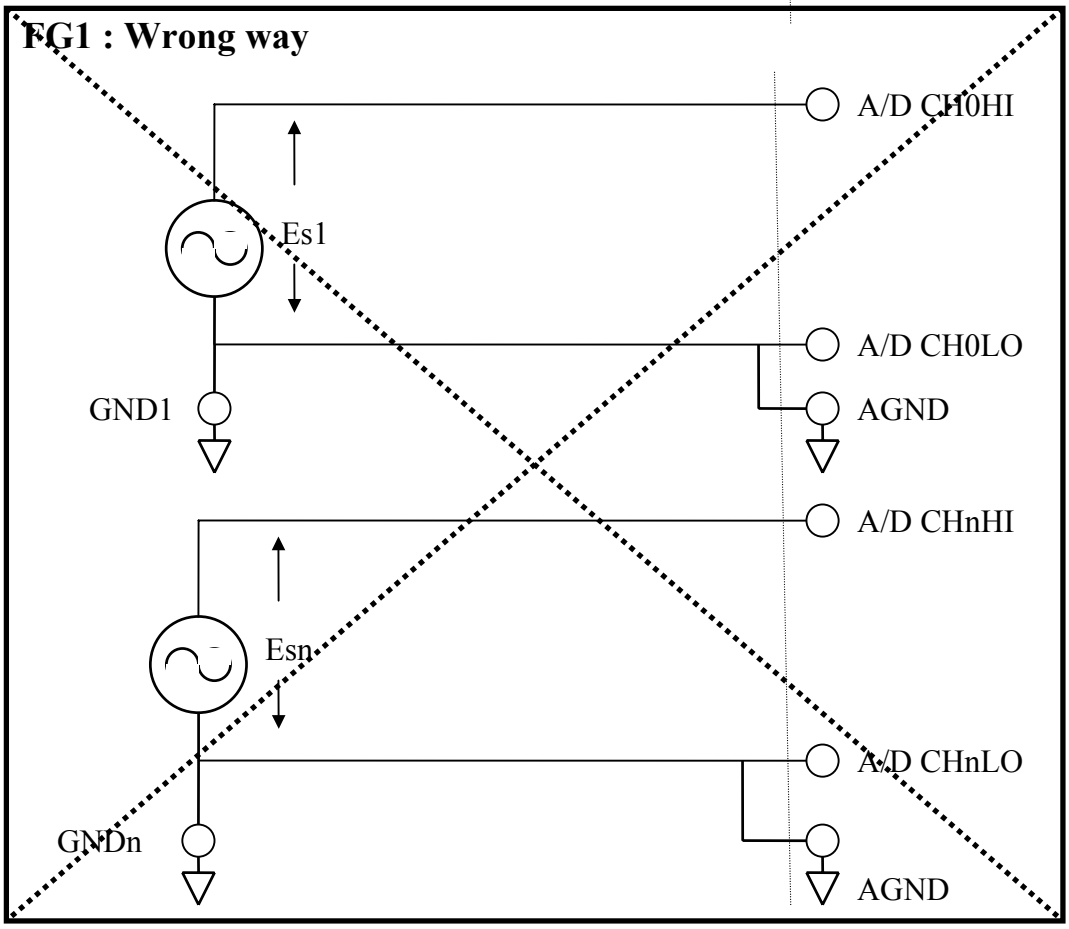
If the user can not make sure the characteristic of input signal, the test steps are given as below:

1. **Step1 : try Fig1 and record the measurement result**
2. **Step2 : try Fig4 and record the measurement result**
3. **Step3 : try Fig2 and record the measurement result**
4. **Compare the measurement result of step1,step2,step3 and select the best one**

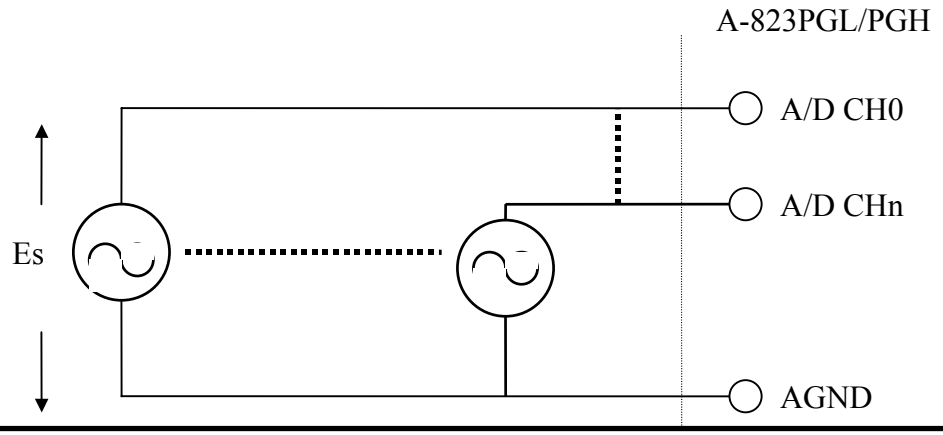
1. FG1 : Connecting to grounding source input (Right way)



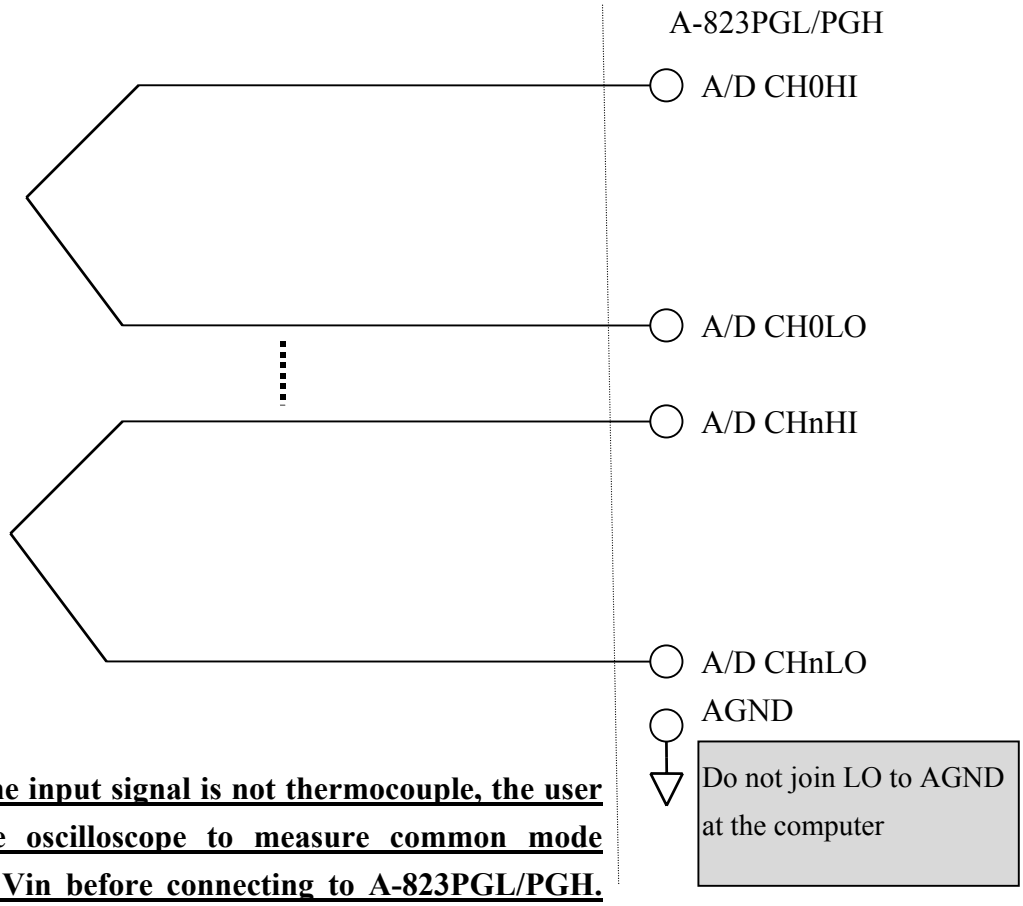
FG1 : Wrong way



FG2 : Connecting to singled-ended input configuration



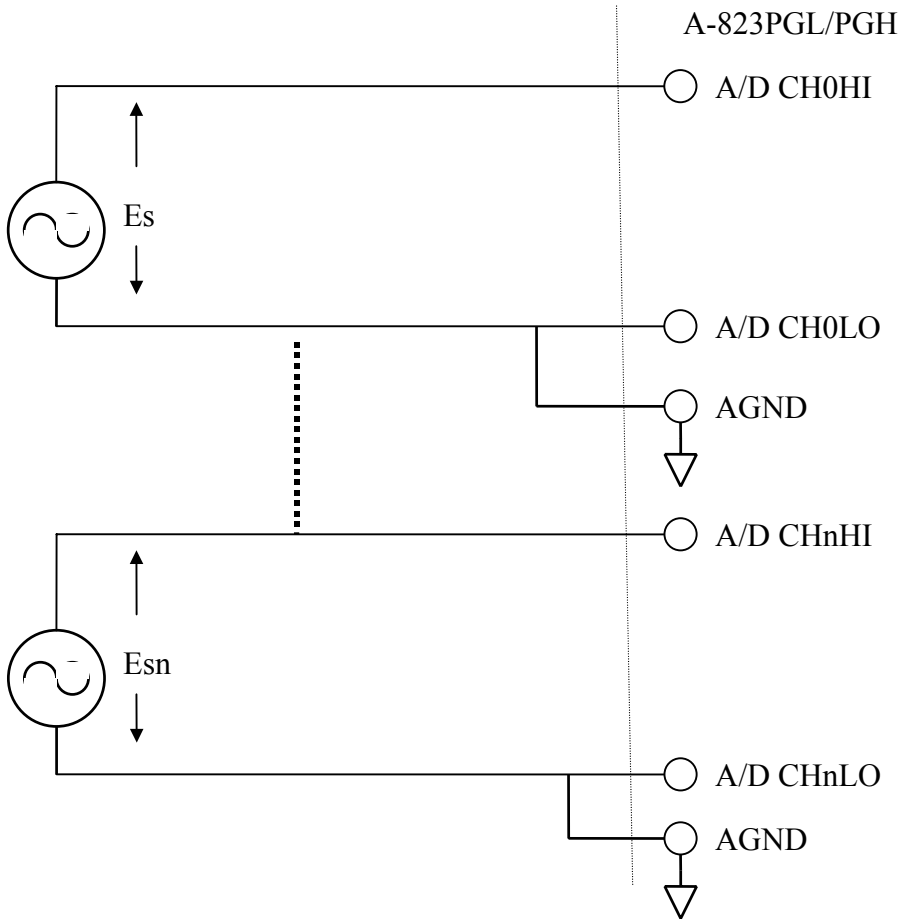
FG3 : connecting to thermocouple configuration



Note : If the input signal is not thermocouple, the user should use oscilloscope to measure common mode voltage of Vin before connecting to A-823PGL/PGH. Don't use voltage meter or multimeter.

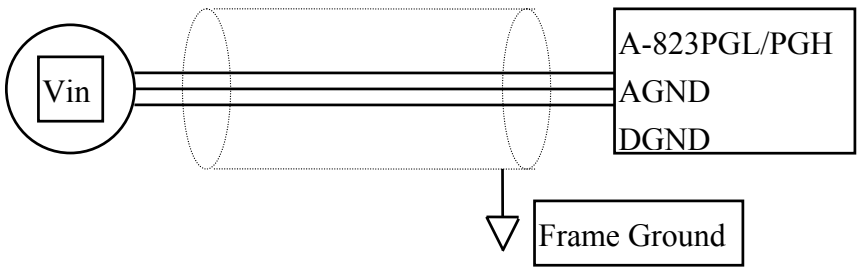
CAUTION : In Fig3, the maximum common mode voltage between the analog input source and the AGND is 70Vp-p, so the user must make sure that the input signal is under specification first. If the common mode voltage is over 70Vp-p, the input multiplexer will be damaged forever.

FG4 : connecting to floating source configuration



Signal Shielding

- Signal shielding connections in Fig1 to Fig4 are all the same
- Use single-point connection to **frame ground (not AGND or DGND)**



2.10 Using DB-8235 CJC Output

The DB-8235 daughter board built-in CJC Circuitry is provided producing 10mV per Deg C With 0.0 Volts @ -273 Deg C. The A-823 Should be protected from draughts and direct sunlight in order to accurately reflect room temperature.

CJC Calibration:

1. Connect the A-823PGL/PGH to DB-8235 CN1
2. Set A-823PGL/PGH to Single-ended Mode
3. set JP1 to 1-2 and JP2 to 2-3 (Single-ended mode)
4. Read the temperature from a digital thermometer placed near D1/D2(See DB-8235 Layout) .
5. Read A-823PGL/PGH analog input channel 0 (single-ended Channel 0)
6. Adjust VR1 Until a stable reading of 10mV per deg C is attained .

For example, when the environment temperature is 24 deg C. the reading value of CJC will be 2.97V

(273 deg c +24 deg c) X 10 mV/deg c = 2.97V

You should need an A/D Channel for CJC calibration. AI0 is reserved for CJC calibration use in single ended mode and CH0-HI & CH0-LO is reserved for differential mode . It is recommended to use differential mode if measuring thermocouple.

3. Connector

The A-823PGL/PGH provides three connectors. Connector 1, **CN1, function as 16 bits digital input.** Connector 2, **CN2, function as 16 digital output**. Connector 3, **CN3, function as analog input, analog output or timer/counter input/output**.

3.1 CN1/CN2/CN3 Pin Assignment

CN1 : Digital Input Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Digital Input 0/TTL	2	Digital Input 1/TTL
3	Digital Input 2/TTL	4	Digital Input 3/TTL
5	Digital Input 4/TTL	6	Digital Input 5/TTL
7	Digital Input 6/TTL	8	Digital Input 7/TTL
9	Digital Input 8/TTL	10	Digital Input 9/TTL
11	Digital Input 10/TTL	12	Digital Input 11/TTL
13	Digital Input 12/TTL	14	Digital Input 13/TTL
15	Digital Input 14/TTL	16	Digital Input 15/TTL
17	PCB‘s GND output	18	PCB‘s GND output
19	PCB‘s +5V output	20	PCB ‘s +12V output

CN2 : Digital Output Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Digital Output 0/TTL	2	Digital Output 1/TTL
3	Digital Output 2/TTL	4	Digital Output 3/TTL
5	Digital Output 4/TTL	6	Digital Output 5/TTL
7	Digital Output 6/TTL	8	Digital Output 7/TTL
9	Digital Output 8/TTL	10	Digital Output 9/TTL
11	Digital Output 10/TTL	12	Digital Output 11/TTL
13	Digital Output 12/TTL	14	Digital Output 13TL
15	Digital Output 14/TTL	16	Digital Output 15/TTL
17	PCB‘s GND output	18	PCB‘s GND output
19	PCB‘s +5V output	20	PCB‘s +12V output

FOR SINGLE-ENDED SIGNAL

CN3 : Analog input/Analog output/Timer/Counter Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Analog Input 0/+	20	Analog Input 8/+
2	Analog Input 1/+	21	Analog Input 9/+
3	Analog Input 2/+	22	Analog Input 10/+
4	Analog Input 3/+	23	Analog Input 11/+
5	Analog Input 4/+	24	Analog Input 12/+
6	Analog Input 5/+	25	Analog Input 13/+
7	Analog Input 6/+	26	Analog Input 14/+
8	Analog Input 7/+	27	Analog Input 15/+
9	PCB‘s analog GND output	28	PCB‘s analog GND output
10	PCB‘s analog GND output	29	PCB‘s analog GND output
11	D/A‘s internal -5V/-10V voltage reference output	30	D/A channel 0‘s analog voltage output
12	D/A channel 1‘s external voltage reference input	31	D/A channel 0‘s external voltage reference input
13	PCB‘s +12V output	32	D/A channel 1‘s analog voltage output
14	PCB‘s analog GND output	33	User timer/counter‘s GATE control input
15	PCB‘s digital GND output	34	Timer/counter 1&2‘s GATE control input
16	User timer/counter‘s output	35	Timer/counter 1‘s output
17	External trigger source input/TTL	36	Reserved
18	Reserved	37	User timer/counter‘s external clock input (internal=2M)
19	PCB‘s +5V output	XXXXXXX	This pin not available

FOR DIFFERENTIAL SIGNAL

CN3 : Analog input/Analog output/Timer/Counter Connector Pin Assignment.

Pin Number	Description	Pin Number	Description
1	Analog Input 0/+	20	Analog Input 0/-
2	Analog Input 1/+	21	Analog Input 1/-
3	Analog Input 2/+	22	Analog Input 2/-
4	Analog Input 3/+	23	Analog Input 3/-
5	Analog Input 4/+	24	Analog Input 4/-
6	Analog Input 5/+	25	Analog Input 5/-
7	Analog Input 6/+	26	Analog Input 6/-
8	Analog Input 7/+	27	Analog Input 7/-
9	PCB‘s analog GND output	28	PCB‘s analog GND output
10	PCB‘s analog GND output	29	PCB‘s analog GND output
11	D/A‘s internal -5V/-10V voltage reference output	30	D/A channel 0‘s analog voltage output
12	D/A channel 1‘s external voltage reference input	31	D/A channel 0‘s external voltage reference input
13	PCB‘s +12V output	32	D/A channel 1‘s analog voltage output
14	PCB‘s analog GND output	33	User timer/counter‘s GATE control input
15	PCB‘s digital GND output	34	Timer/counter 1&2‘s GATE control input
16	User timer/counter‘s output	35	Timer/counter 1‘s output
17	External trigger source input/TTL	36	Reserved
18	Reserved	37	User timer/counter‘s external clock input (internal=2M)
19	PCB‘s +5V output	XXXXXXX	This pin not available

3.2 Daughter Board

The A-823PGL/PGH can be connected with many different daughter boards. The function of these daughter boards are described as follows.

3.2.1 DB-8235

The DB-8235 (or ACLD-8125) provides a **on-board CJC**(Cold Junction Compensation) circuit for thermocouple measurement and **terminal block** for easy signal connection and measurement . The CJC is connected to A/D channel_0. The A-823PGL/PGH can connect CN3 direct to DB-8235 through a 37-pin D-sub connector.

3.2.2 DB-37

The DB-37 (or ACLD-9137)is a **general purpose** 37-pin connector. This board direct connect to a 37-pin D-sub connector. It is suitable for easy signal connection and measurement.

3.2.3 DB-16P

The DB-16P(or 782 series) is a **16 channel isolated digital input** board. The A-823PGL/PGH provides 16 channel non-isolated TTL-compatible digital inputs from CN1. If connecting to DB-16P, the A-823PGL/PGH can provide 16 channel isolated digital input signals. Isolation can protect PC if abnormal input signal is occurred.

3.2.4 DB-16R

The DB-16R(or 785 series) provides **16 channel SPDT relay output.** The A-823PGL/PGH provides 16 channel TTL-compatible digital output from CN2. If connecting to DB-16R, the A-823PGL/PGH can provide 16 channel relay output to control power device.

4. Calibration

The A-823PGL/PGH is calibrated to its best state of operation. For environment with large vibration, recalibration is recommended. Before calibrating the A-823PGL/PGH, user should take care the following issue:

- One 6 digit multimeter
- One stable voltage source (4.9988V)
- Diagnostic program : this program included in the delivered package will guide the user to proceed the calibration.

4.1 Calibration VR Description

There are seven VRs on the A-823PGL/PGH. Calibration need to adjust all seven VRs.

VR Num.	Description
VR1	A/D‘s offset adjustment
VR2	A/D‘s gain adjustment
VR3	D/A channel 0‘s gain adjustment
VR4	D/A channel 1‘s gain adjustment
VR5	D/A‘s reference voltage adjustment
VR6	A/D unipolar‘s offset adjustment
VR7	A/D programmable amplifier‘s offset adjustment
VR8	D/A CH1 Bipolar’s offset adjustment
VR9	D/A CH0 Bipolar’s offset adjustment

4.2 D/A Calibration Steps

D/A unipolar calibration

1. Run A-823DIAG.EXE
2. Press “Right Arrow Key” to select “CALIBRATION” item
3. Press “Down Arrow Key” to select “G. D/A REFERENCE” item.
4. Press “Enter Key”
5. Connect VREF, pin 11 of CN3, to DVM (DC Voltage Meter)
6. Adjust VR5 until DVM=4.9988V
7. Press “ESC Key”
8. Select & Execute “A. D/A REFERENCE 1” item
9. Connect D/A channel 0, pin 30 of CN3, to DVM
10. Adjust VR3 until DVM=4.9988V
11. Press “ESC Key”
12. Select & Execute “B. D/A REFERENCE2” item
13. Connect D/A channel 1, pin 32 of CN3, to DVM
14. Adjust VR4 until DVM=4.9988V

D/A Bipolar calibration

15. When the D/A unipolar calibration is ready.
16. Setting JP9/JP10 to Bipolar mode (JP9 for D/A CH0 , JP10 for D/C CH1)
17. Write 0x0800 to D/A CH0 then adjust VR8 until D/A CH0 output 0V
18. Write 0x0800 to D/A CH1 then adjust VR9 until D/A CH1 output 0V

4.3 A/D Calibration Steps

1. Run A-823DIAG.EXE
2. Press “Right Arrow Key” to select “CALIBRATION” item
3. Press “Down Arrow Key” to select “C. A/D REFERENCE” item.
4. Press “Enter Key”
5. Input stable 4.9988V to A/D channel 0, pin 1 of CN3
6. Adjust VR2 until A/D data shown in screen between 4094 to 4095
7. Press “ESC Key”
8. Select & Execute “D. A/D OFFSET” item
9. Input stable 0V to A/D channel 0, pin1 of CN3
10. Adjust VR1 until A/D data shown in screen between 2048 to 2049
11. Press “ESC Key”
12. Repeat step_3 to step_11 until no need to adjust VR2,VR1
13. Select & Execute “E. PGA OFFSET” item
14. Input stable 0V to A/D channel 0, pin 1 of CN3
15. Adjust VR7 until A/D data shown in screen between 2048 to 2049
16. Press “ESC Key”
17. Select & Execute “F. PGA REFERENCE” item
18. Input stable 0V to A/D channel 0 , pin1 of CN3
19. Adjust VR6 until A/D data shown in screen between 0 to 1

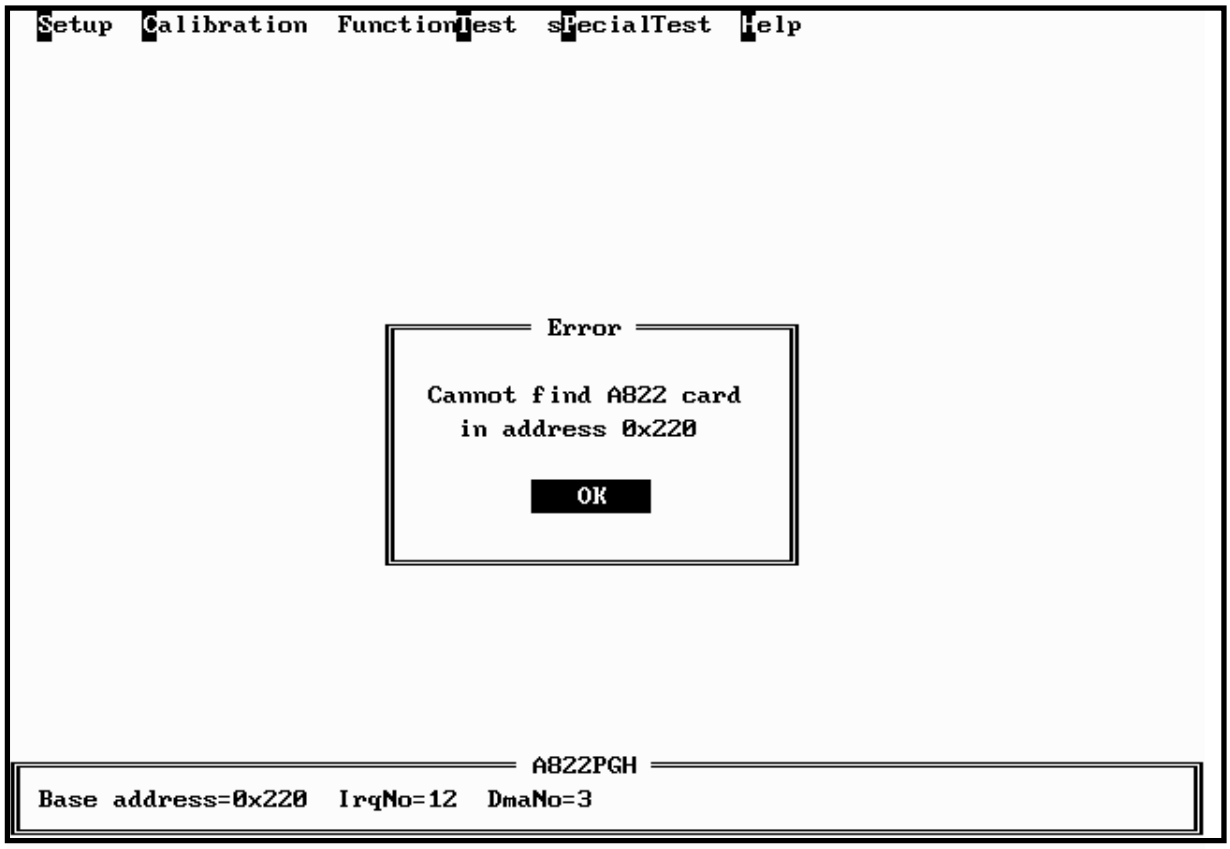
5. Diagnostic Utility

5.1 Introduction

The diagnostic utility, A-823DIAG.EXE, is a menu-driven program which give you complete testing of the A-823PGL/PGH board. When you doubt the operation of A-823PGL/PGH board, run the diagnostic utility to check the function of the board. To run the diagnostic utility, change to the sub directory used in the installation process (C:\A-823 for example). Then typing "A-823DIAG" <Enter> to start. These steps are shown as following:

C:\>CD A-823 <Enter>
C:\A-823>CD DIAG <Enter>
C:\A-823\DIAG>A-823DIAG <Enter>

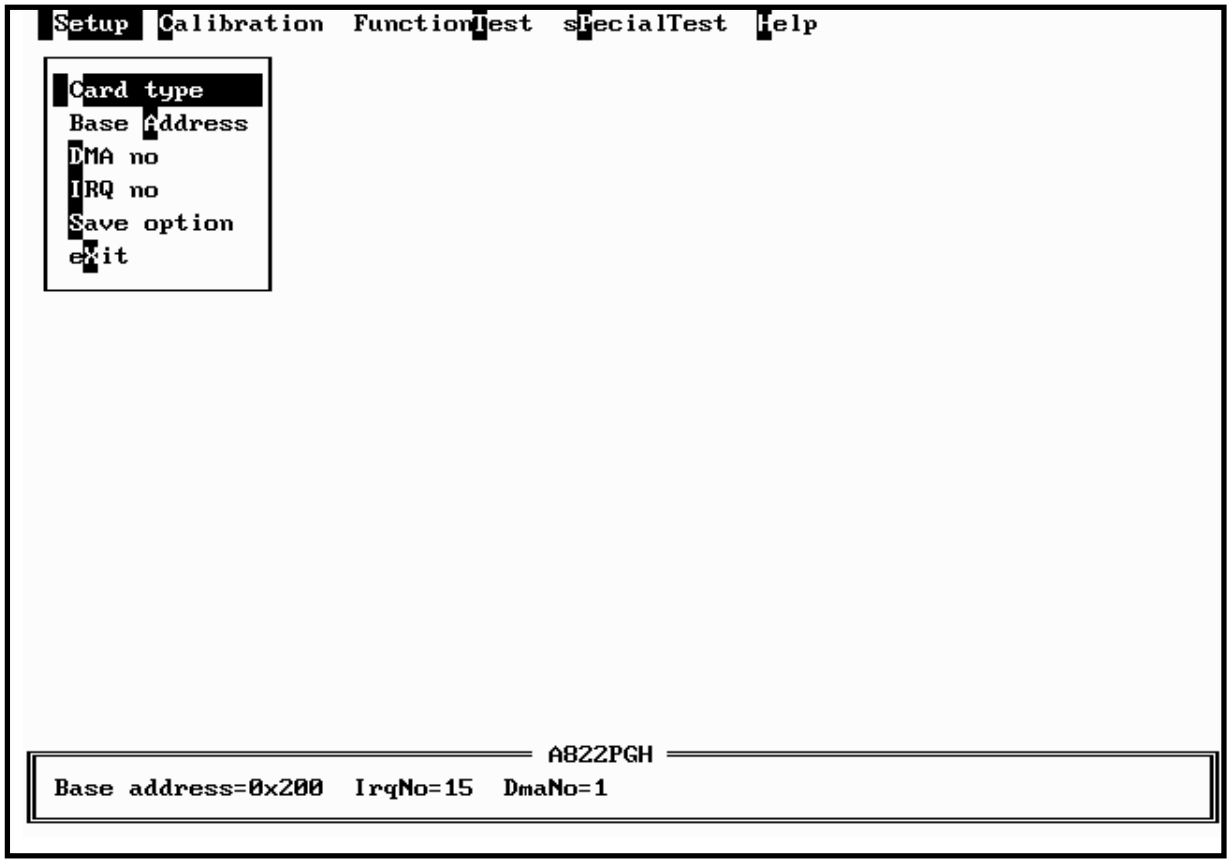
A configuration file, named A-823.CFG, associated with the A-823DIAG.EXE. The configuration of the A-823PGL/PGH board is recorded in this file. The information includes the board's I/O base address, interrupt number and DMA channel number used by A-823PGL/PGH. During A-823DIAG running, if you do some adjustment , the change will not be saved automatically. So the user must select the save function to save the changes. When the A-823DIAG.EXE beginning, it will automatically check if the jumper setting of I/O base address is identical to the value stored in configuration file. If the address is not identical, a error message will appear to warn you. The screen is shown as below.



Although you can continue the A-823DIAG by press any key, it is recommended to correct this situation by setting the proper jumper setting. Because many operation in the A-823DIAG, the I/O base address is check firstly. And it don't work if the error occurs

5.2 Running The Diagnostic Utility

The initialization screen of A-823DIAG shown as below. As you can see, there are five main menu in the initialization screen. They are Setup, Calibration, FunctionTest, sPecialTest and Help. Using the Left or Right key to select the main menu. A main menu with highlight means it is selected, and some menu items are associated with it. Then using the Up or Down key to select the menu item, also the selected menu item will be highlighted. Alternately, the user can press the command key to highlight the menu item. A command key in a menu item is the character which is highlighted. To proceed a function associated the highlighted menu item, just press <Enter>. And to press <Esc> to abort the current function.

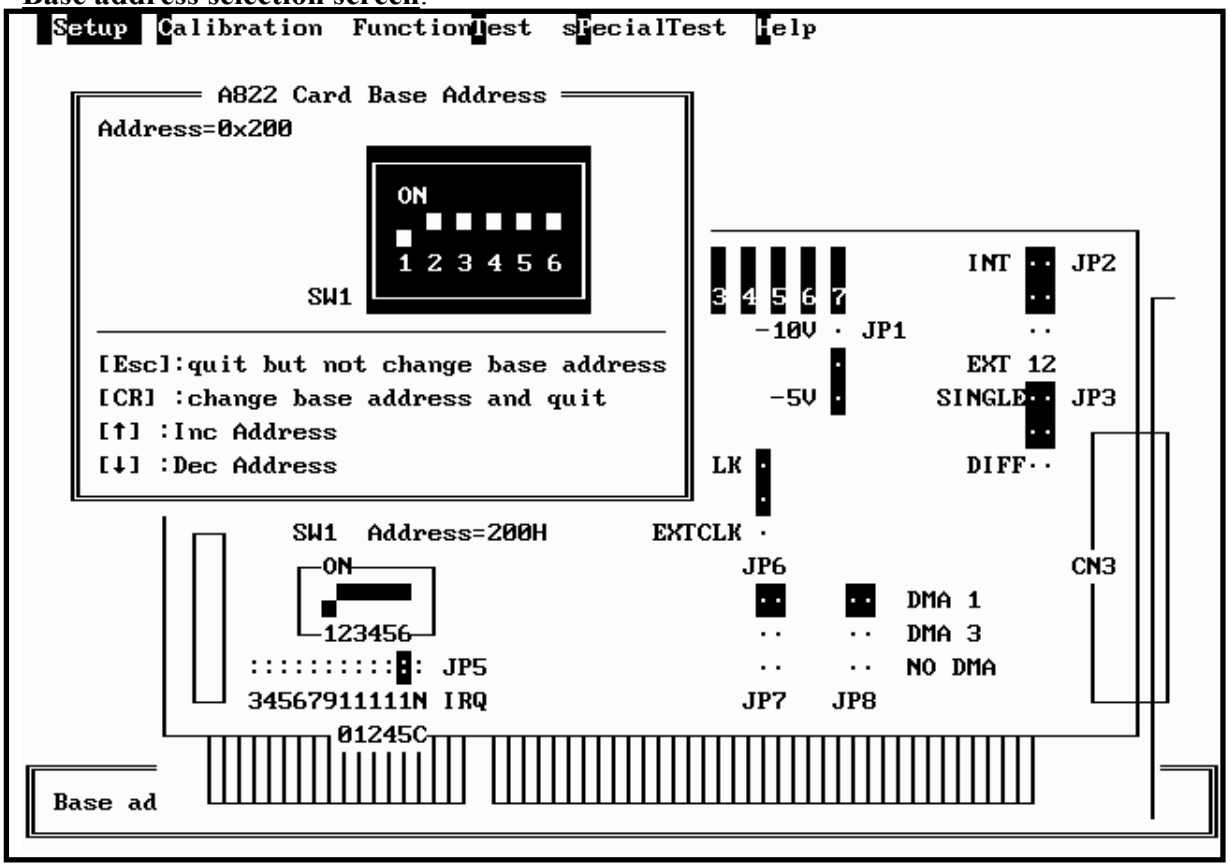


5.2.1 Setup

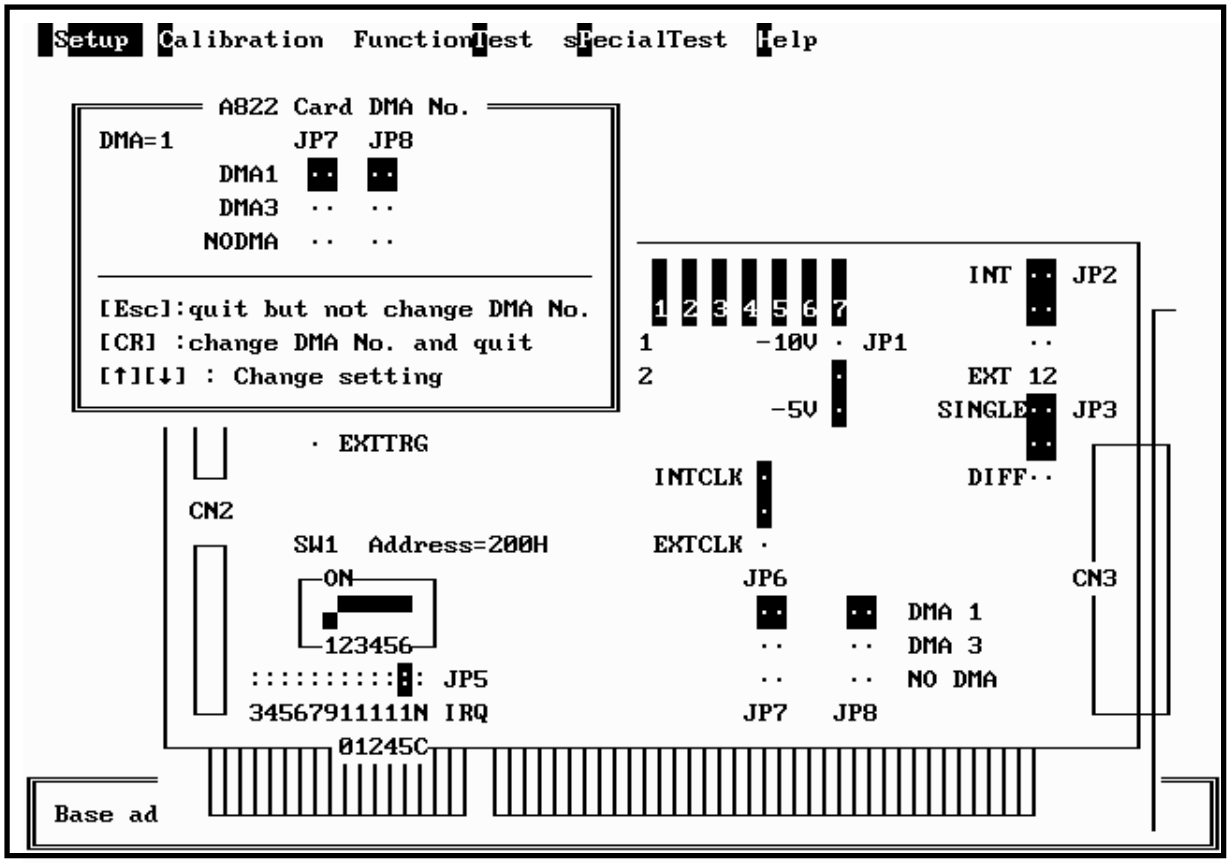
The Setup main menu allow user to setup the board configuration. There are six functions in this item, Card type, Base Addresss, DMA no, IRQ no, Save option, eXit.

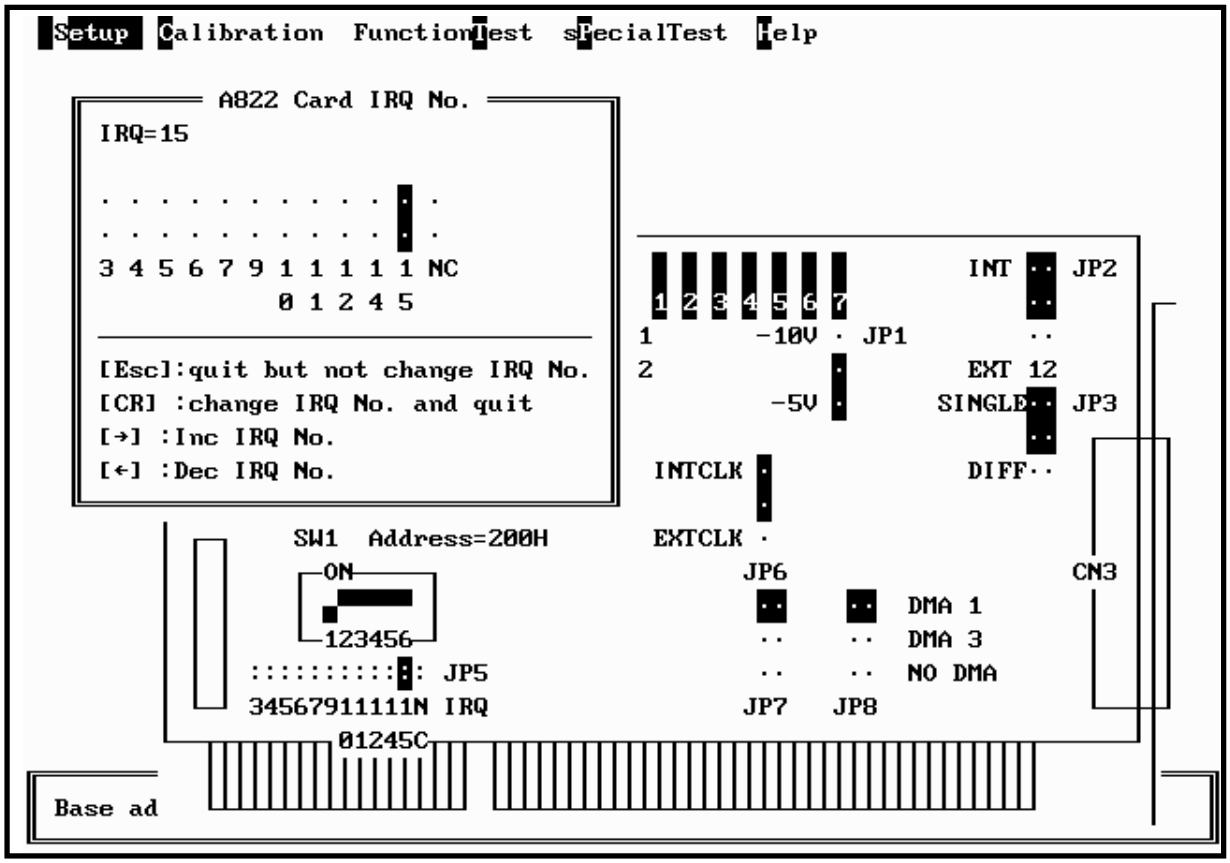
Card type : **<Up/Down>** key to select A-823PGL/PGH, **<Enter>** key to select
Base Address : **<Up/Down>** key to select base address, **<Enter>** key to select
DMA no : <**Up/Down>** key to select DMA no, **<Enter>** key to select
IRQ no : <**Left/Right>** key to select IRQ no, **<Enter>** key to select
Save option : <**Left/Right>** key to select yes/no, **<Enter>** key to select
eXit : <**Left/Right>** key to select yes/no, **<Enter>** key to select

Base address selection screen.



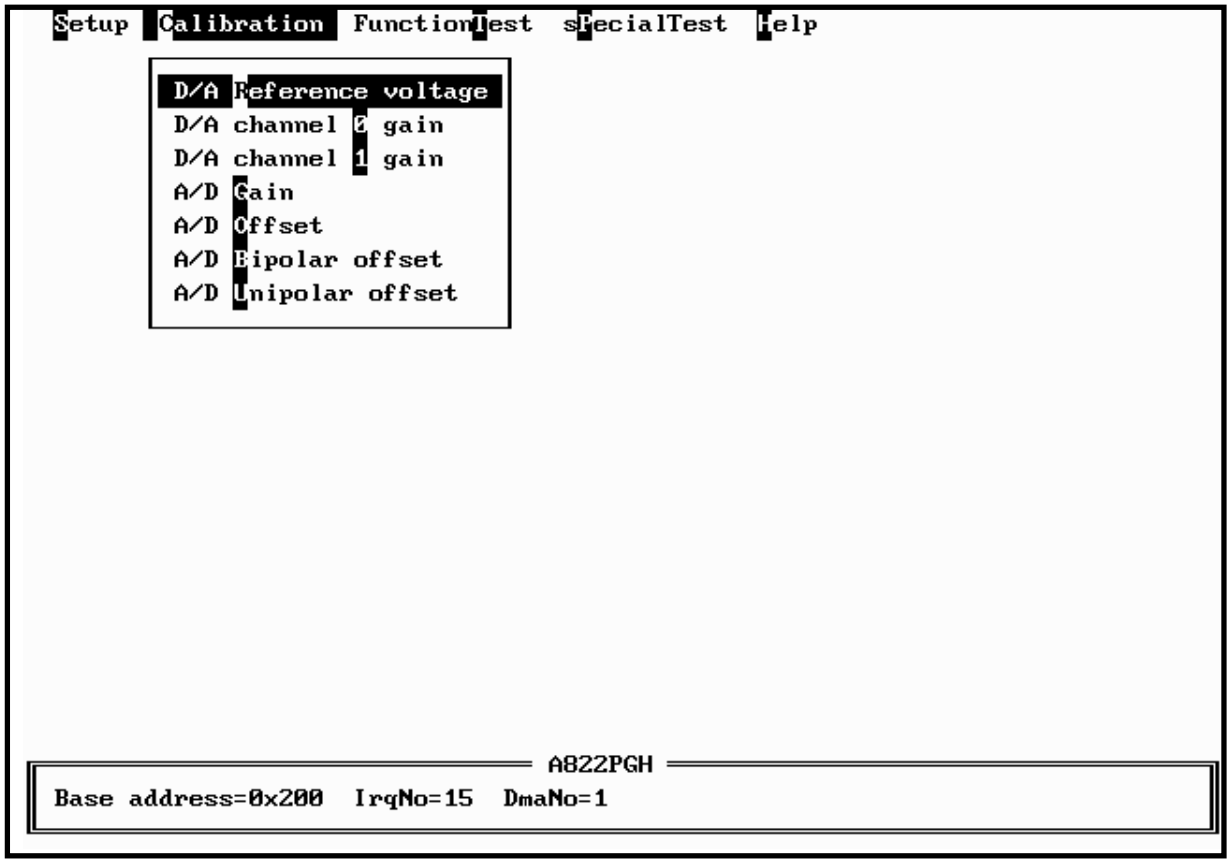
DMA no and IRQ no selection screen





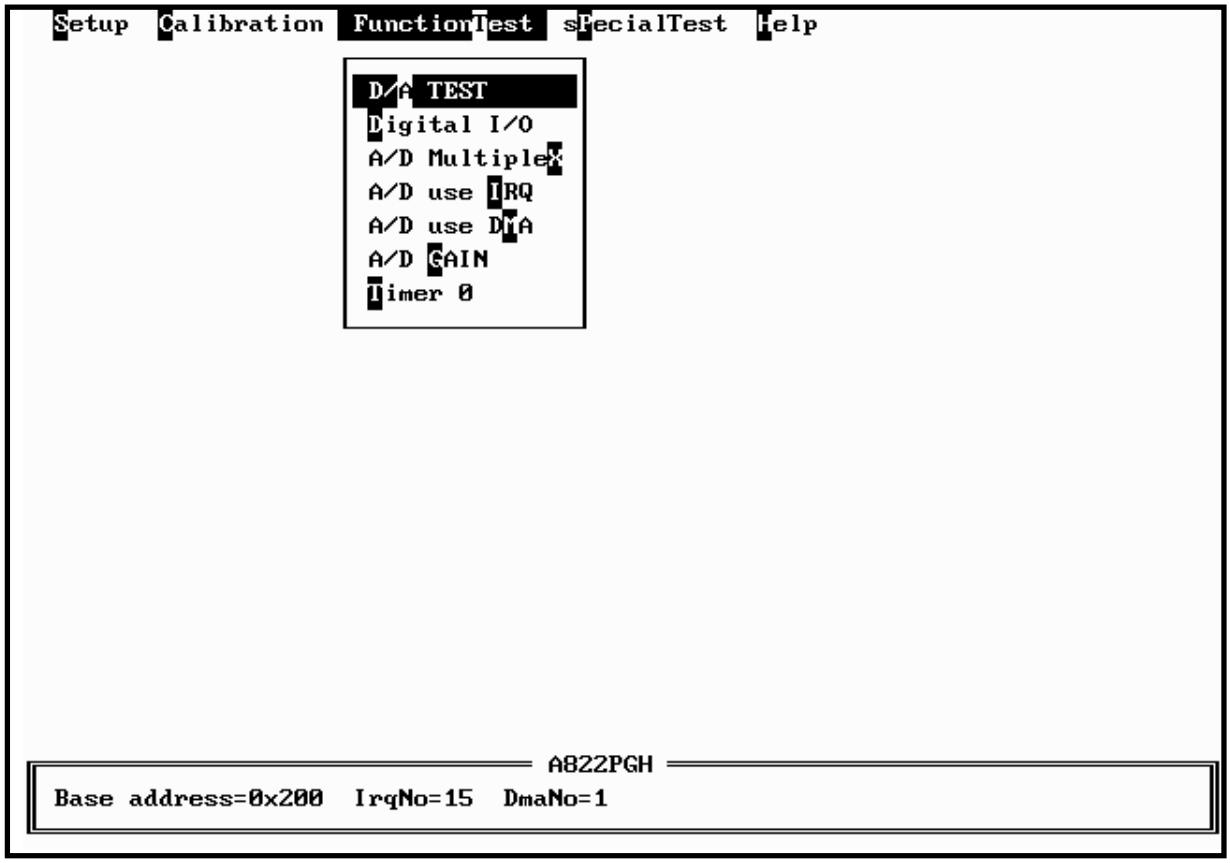
5.2.2 CALIBRATION

The CALIBRATION main menu contains ten menu items: those are, D/A Reference voltage, D/A Channel 0 gain, D/A channel 1 gain, A/D Gain, A/D Offset, A/D Bipolar Offset, A/D Unipolar Offset. These items are about calibration the A-823PGL/PGH. CALIBRATION main menu, a graphic presentation of the A-823PGL/PGH board's layout shown. The calibration will become as a visual process to release user's effort. To keep the optimal performance and correct precision for the board , it is needed to calibrate the board after working a long time period. There are seven VRs need to be tuned in calibration process. When you highlight one of the first seven menu item, the associated VR is blinking . And a message window will appear to indicate you how to tune the VRs. The main menu screen is shown as below.



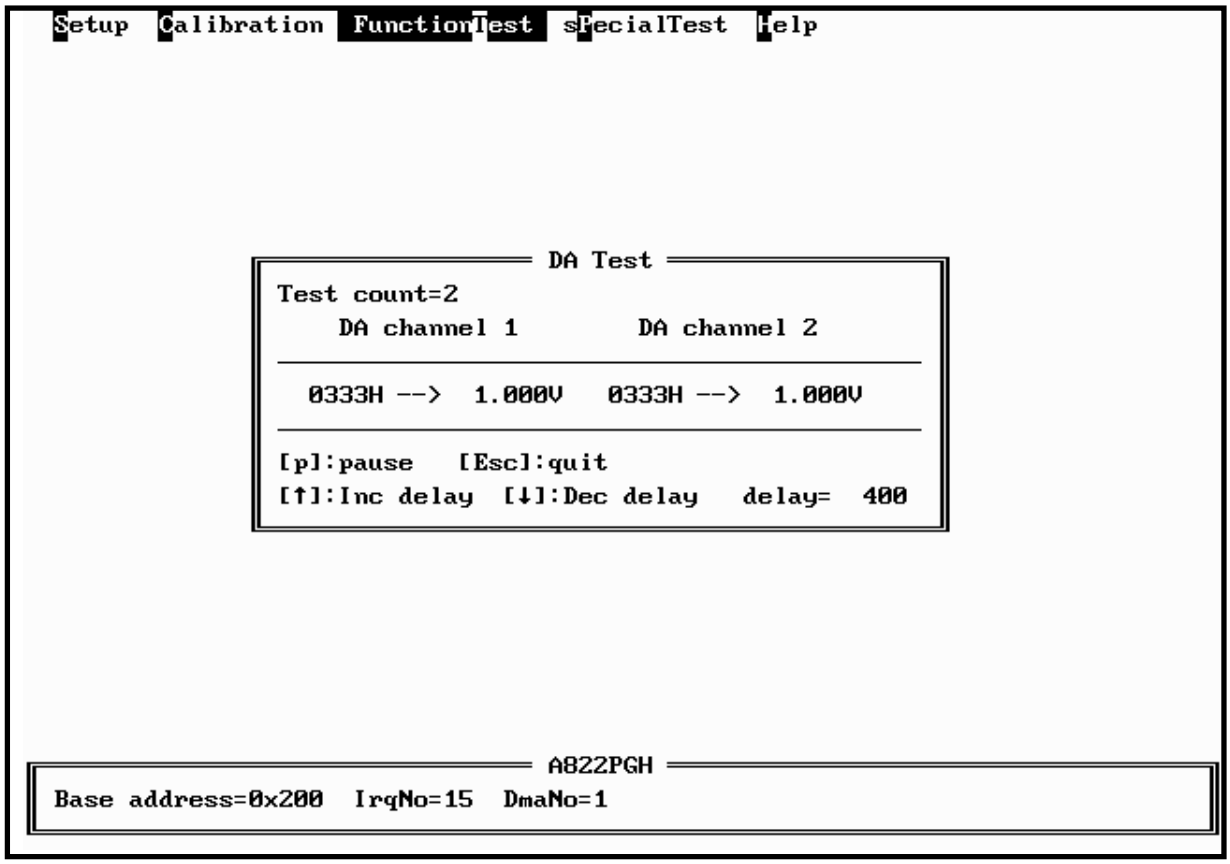
5.2.3 FUNCTION TEST

The FUNCTION TEST main menu contains seven menu items: those are D/A TEST, Digital I/O, A/D MULTIPLEX, A/D use IRQ, A/D use DMA, A/D GAIN, Timer 0. The main memu is shown as below.



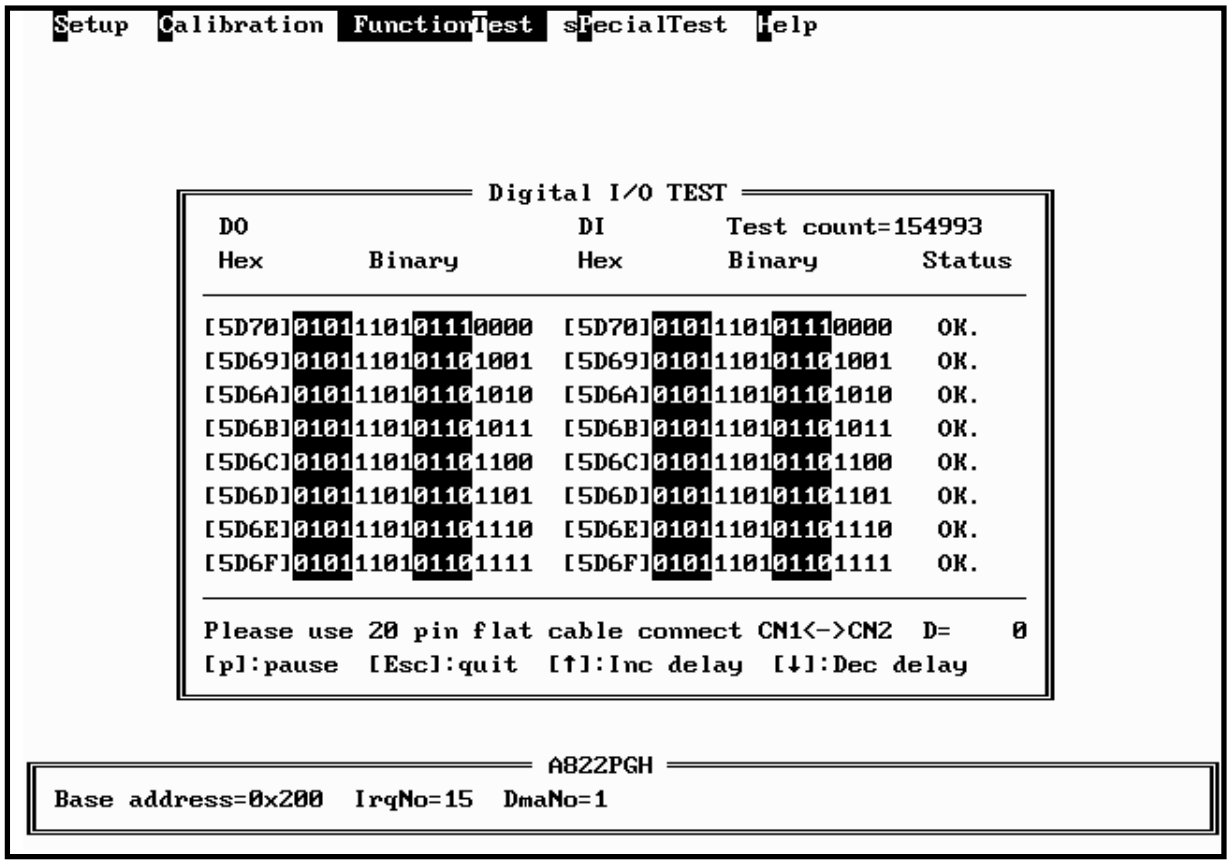
If selecting “D/A TEST” item, the screen is shown as below.

<D/A TEST > test screen



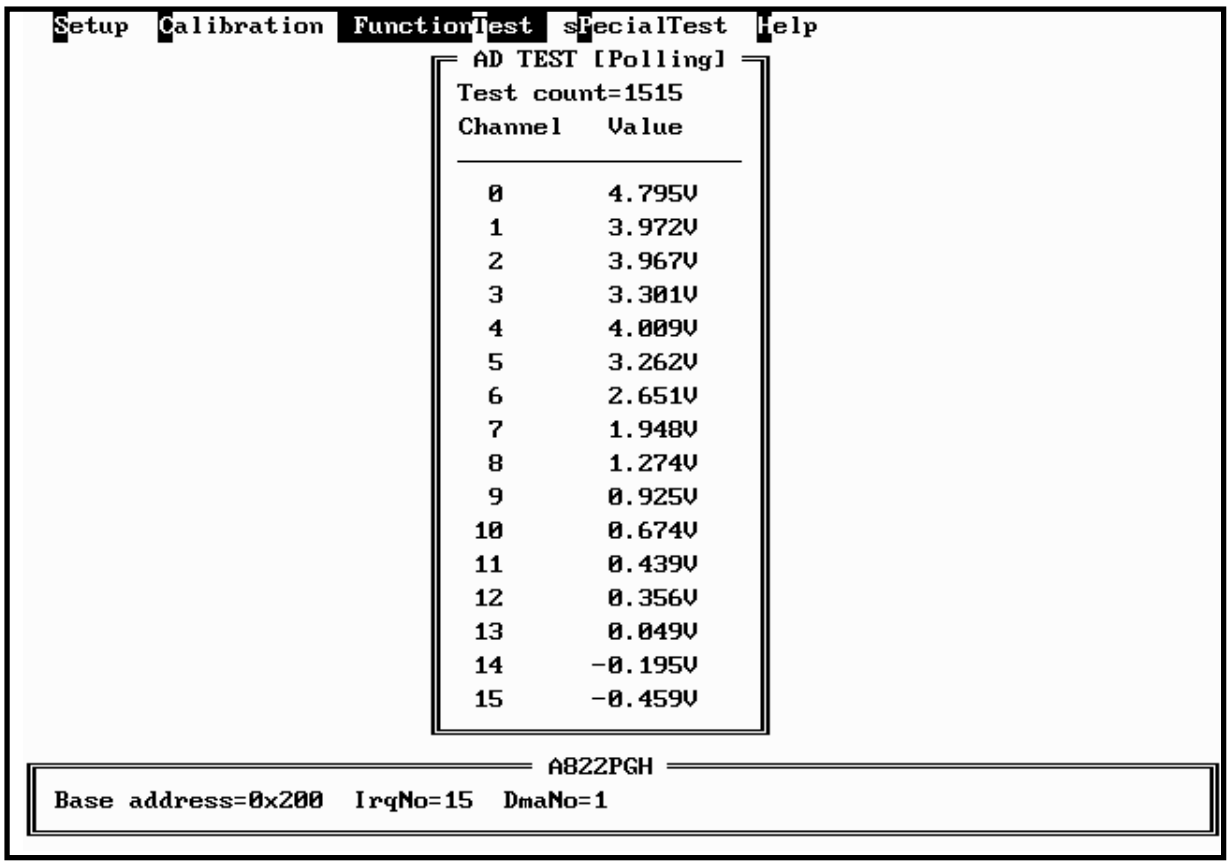
- assume D/A output range 0 ~ 5V
- send D/A output to both channels simultaneously
- press <p> pause screen, press <p> again release screen
- press <Up> key to increase screen delay
- press <Down > key to delay screen delay
- press <ESC> key to quit

<Digital I/O> test screen



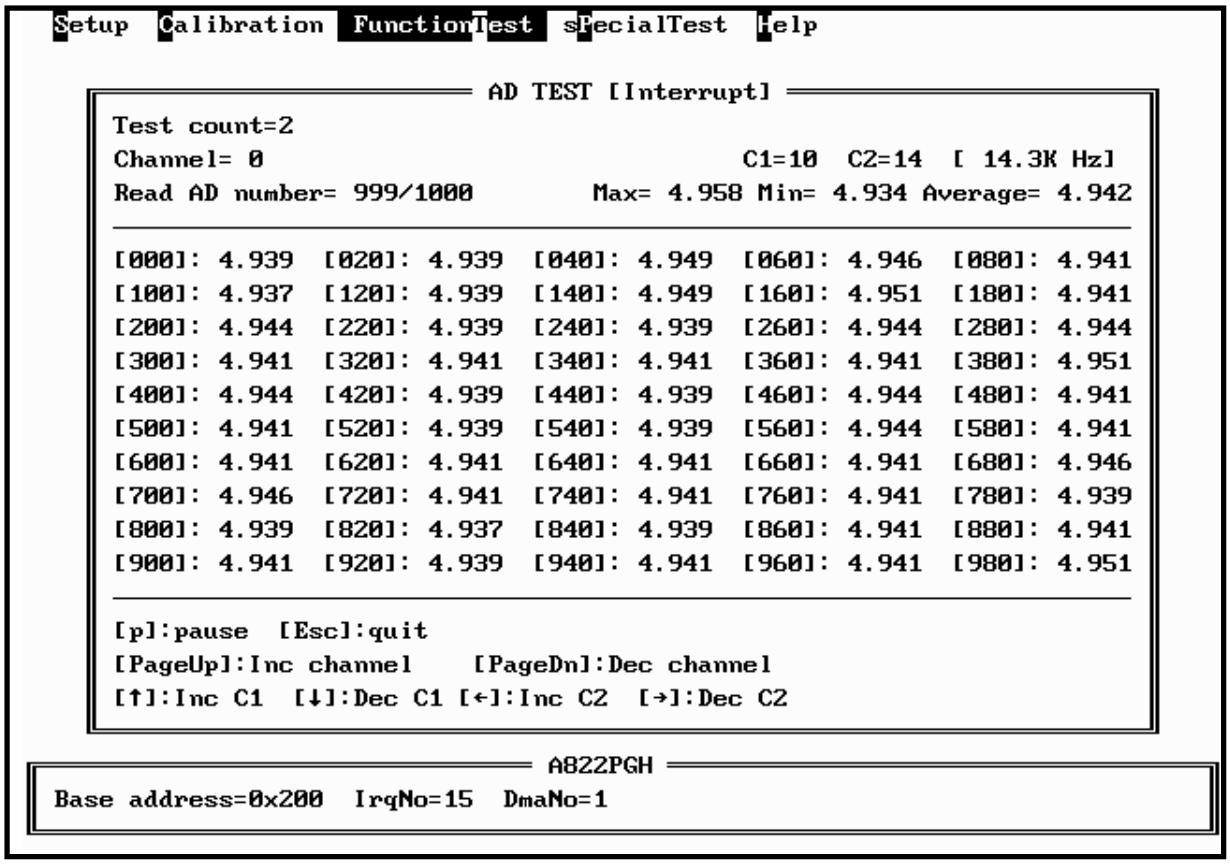
- assume CN1 direct connect to CN2
- a 16 bits up counter is send to 16 channel DO
- 16 channel DO direct connect to 16 channel DI
- 16 channel DI are readback and show in screen
- DO == DI → show OK in screen
- DO != DI → show Error in screen
- press <p> pause screen, press <p> again release screen
- press <Up> key to increase screen delay
- press <Down > key to delay screen delay
- press <ESC> key to quit

<A/D Multiplexer> test screen



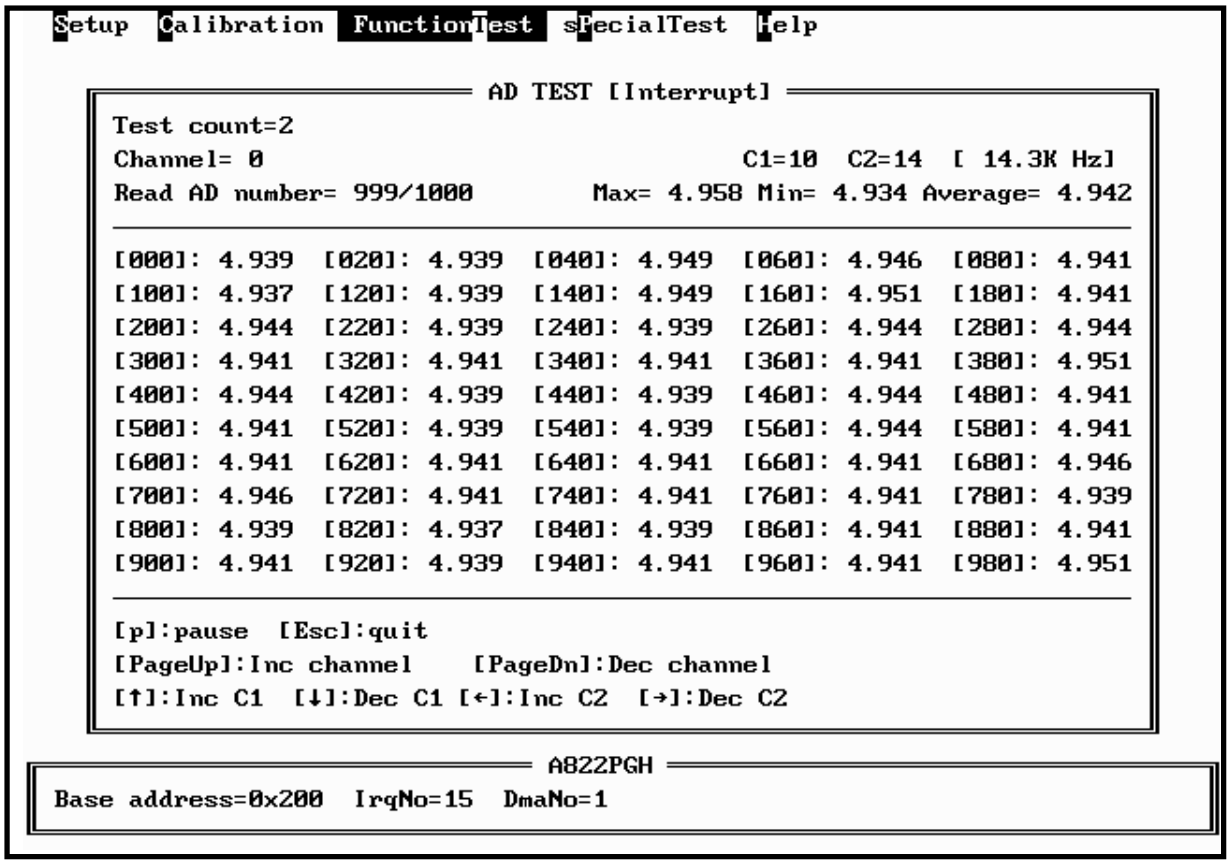
- assume 16 channel single-ended, bipolar, gain=1, analog input signals
- input range from -5V to +5V
- continue scan between 16 channel
- press <ESC> key to quit

<A/D use IRQ> test screen



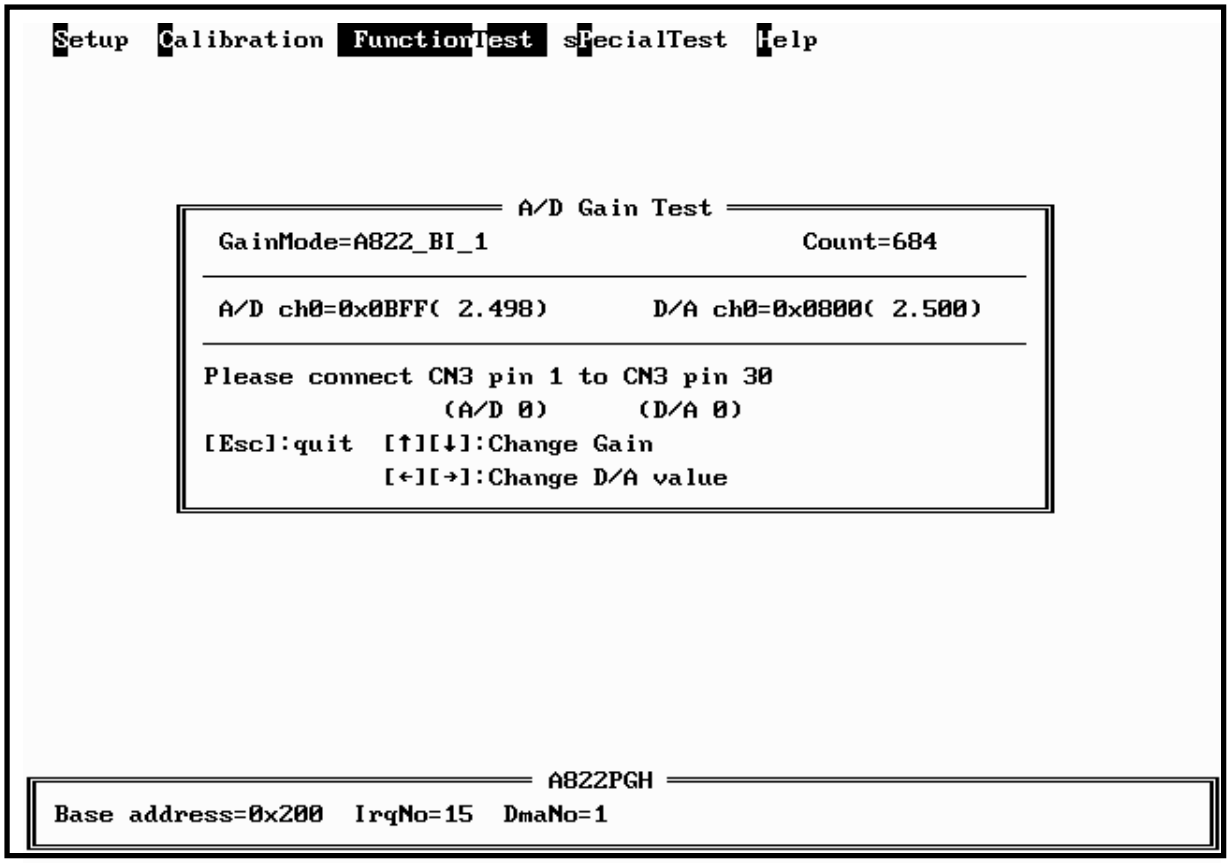
- assume single-ended, bipolar, gain=1
- use <PgUp> key to select the next channel
- use <PgDn> key to select the previous channel
- use <Up>/<Down> key to adjust C1
- use <Left>/<Right> key to adjust C2
- sampling rate = pacer timer rate = 2000/(C1*C2) K
- use <p> key to pause screen, use next <p> key to release screen
- use <ESC> to quit
- A/D mode control register=0x06 → select pacer trigger and use interrupt transfer
- one cycle sample 1000 A/D data continue
- minimal/maximal/average value shown in screen

<A/D use DMA> test screen



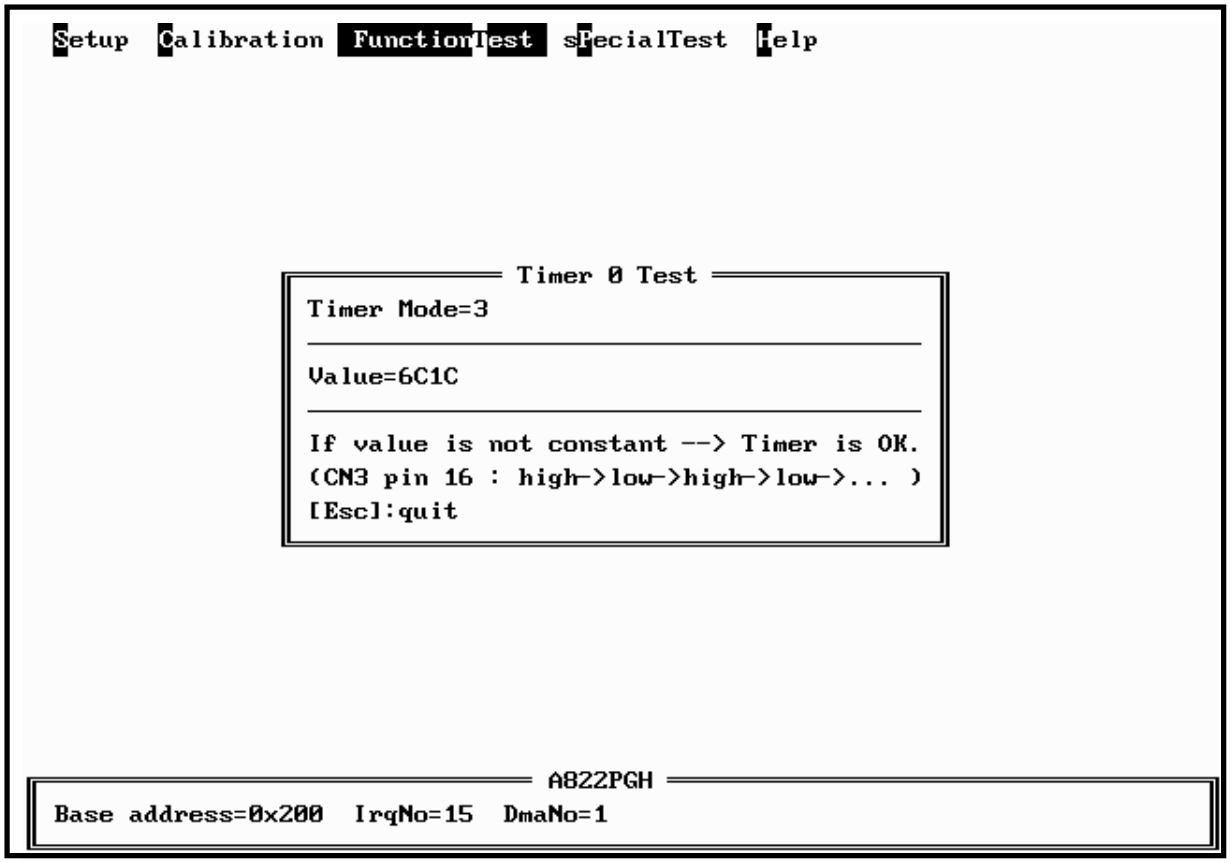
- assume single-ended, bipolar, gain=1
- use <PgUp> key to select the next channel
- use <PgDn> key to select the previous channel
- use <Up>/<Down> key to adjust C1
- use <Left>/<Right> key to adjust C2
- sampling rate = pacer timer rate = 2000/(C1*C2) K
- use <p> key to pause screen, use next <p> key to release screen
- use <ESC> to quit
- A/D mode control register=0x02 → select pacer trigger and use DMA transfer
- one cycle sample 1000 A/D data continue
- minimal/maximal/average value shown in screen

<DA GAIN> test screen



- assume single-ended, bipolar, gain=1, A/D channel 0 connect to D/A channel 0
- use <Up>/<Down> key to adjust gain control code
- use <Left>/<Right> key to adjust D/A output value
- use software trigger and polling transfer mode
- press <ESC> key to quit

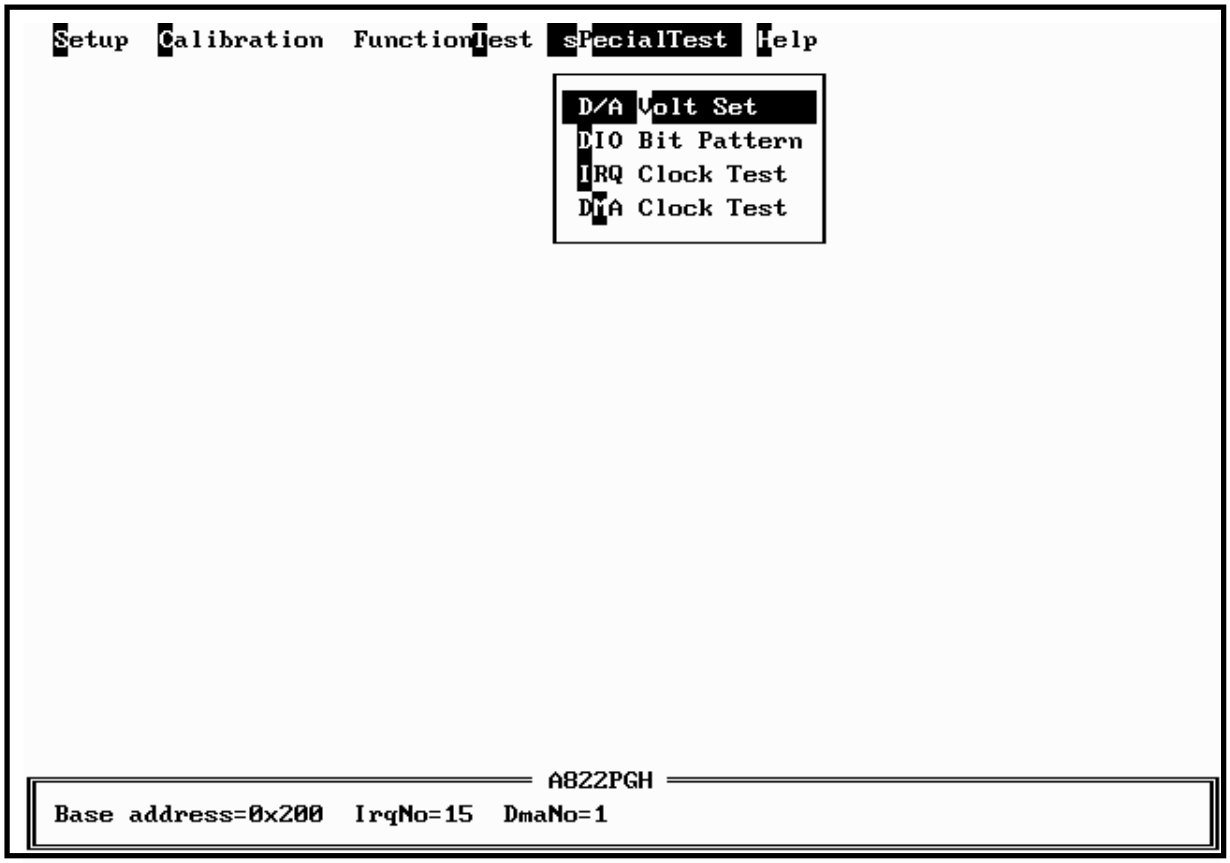
<Timer 0> test screen



- assume JP6 select internal 2M clock
- If the counter0 is normal, the value will increment automatically. If the value is a fixed value, the counter0

5.2.4 SPECIAL TEST

The SPECIAL TEST main menu contains four menu items: those are D/A Volt Set, DIO Bit Pattern, IRQ Clock Test and DMA Clock Test. These functions are reserved for factory testing.



5.2.5 Help

The Help menu will show the software version as below.