PCI-D64HU

User's Manual

Warranty

All products manufactured by ICP DAS are warranted against defective materials for a period of one year from the date of delivery to the original purchaser.

Warning

ICP DAS assume no liability for damages consequent to the use of this product. ICP DAS reserves the right to change this manual at any time without notice. The information furnished by ICP DAS is believed to be accurate and reliable. However, no responsibility is assumed by ICP DAS for its use, nor for any infringements of patents or other rights of third parties resulting from its use.

Copyright

Copyright 2009 by ICP DAS. All rights are reserved.

Trademark

The names used for identification only may be registered trademarks of their respective companies.

Table of Contents

1. Introduction

1.1. General Description

The PCI-D64HU card provides 40 MB/s High-Speed 32-CH Digital Input and 32-CH Digital Output.PCI-D64HU is a high-speed digital I/O card consisting of 32 digital input channels and 32 digital output channels. High-performance designs make this card perfect for high-speed data transfer and pattern generation applications.

The PCI-D64HU has the Card ID switch on board. Users can set Card ID on a board and recognize the board by the ID via software when using two or more PCI-D64HU cards in one computer.

The PCI-D64HU performs high-speed data transfer by bus-mastering DMA via 32-bit PCI bus. The maximum data transfer rate can be up to 40 MB per second. Several digital I/O transfer modes are supported, such as direct programmed I/O control, timer pacer control, external clock mode and handshaking mode. It is a reliable and cost-effective connection interface that works on your computer system to control high-speed peripherals.
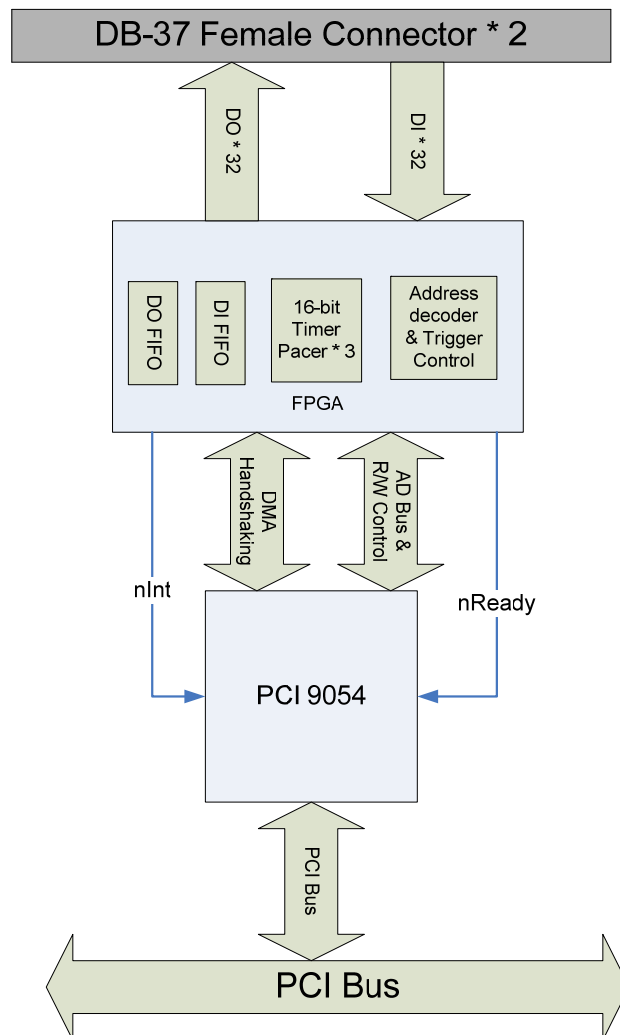
1.2. Features

The following is a list of general features for the PCI-D64HU. Check section 1.5 for more details.

- Support 32-bit, 33 MHz Universal PCI bus
- 32-CH 5V TTL Digital Inputs and 32-CH 5V TTL Digital Outputs
- 2-CH Bus Mastering Scatter/Gather DMA
- Data Transfer Rate up to 40 MB/s for Each Channel
- Support 4 Data Transfer Modes
  - Direct Program Control Mode
  - Internal Timer Pacer Mode
  - External Clock Mode (DI Only)
  - Handshaking Mode
- On Board 1 k/2 k DWORD FIFO for DI/DO Respectively
  DO FIFO Support Ring Buffer Mode -- No Bus Loading in Repetitive Pattern
- Card ID function

1.3. Generation Application

- Programmable Input Digital Filter for All Input Signals Including Handshaking and Trigger Signals

1.4. Block Diagram

DB-37 Female Connector * 2

DO * 32

DI * 32

DO FIFO

DI FIFO

16-bit Timer Pacer * 3

Address decoder & Trigger Control

FPGA

DMA Handshaking

AD Bus & R/W Control

nInt

nReady

PCI 9054

PCI Bus

PCI Bus

1.5. Specifications

Model Name	PCI-D64HU
Digital Input	
Channels	32
Compatibility	5 V/TTL
Input Voltage	Logic 0: 0.8 V max. Logic 1: 2.0 V min.
Handshaking Signals	I_REQ input , I_ACK output , I_TRG input
Digital Output	
Channels	32
Compatibility	5 V/TTL
Output Voltage	Logic 0: 0.55 V max. Logic 1: 2.0 V min.
Output Capability	Sink: 64 mA @ 0.55 V Source: -32 mA @ 2.0 V
Handshaking Signals	O_REQ output, O_ACK input, O_TRG output
Transfer Speed	40 MB/sec for DI and DO simultaneously (max.)
Programmable Digital Filter	
Applicable Signals	All input signals (including 32 DI signals, I_REQ, I_TRG and O_ACK)
Max. removable noise width	(1 ~ 127) x 25 ns
Programmable Pulse Extender	
Applicable Signals	O_REQ
Pulse width	(2 ~ 256) x 25 ns
Timer/Counter	
Channels	3
Resolution	16-bit
Input Frequency	2.5 ~ 20 MHz
Timer 0	Clock source of DI
Timer 1	Clock source of DO
Timer 2	Base clock of Timer 0 and Timer 1
Interrupt	
Sources	O_ACK, I_REQ, Timer 0, Timer 1 and Timer 2
On Board FIFO	
DI / DO	1 k DWORD (32-bit) 2 k DWORD (32-bit)
Size in Ring Buffer Mode	2 ~ 2 k DWORD (32-bit), DO only
General	
Bus Type	Universal PCI, 32-bit, 33 MHz
Card ID	Yes (4-bit)
I/O Connector	Female DB37 x 1 40-pin Box header x 1
Dimensions (L x W x D)	120 mm x 105 mm x 22 mm
Power Consumption	200 mA @ +5 V typical (output no load)
Operating Temperature	0 ~ 60 °C
Storage Temperature	-20 ~ 70 °C
Humidity	5 ~ 85% RH, non-condensing

1.6. Product Check List

In addition to this manual, the package includes the following items:

- One PCI-D64HU card
- One ICP-DAS software CD-ROM
- One Quick Start Guide

It is recommended to read the Quick Start Guide first. The following important information will be given in the Quick Start Guide:

1. Where you can find the software driver & utility
2. How to install software & utility
3. Location of the diagnostic program

1.7. Ordering Information

Ordering Information:

- PCI-D64HU: 40 MB/s High-speed 32-CH DI and 32-CH DO Universal PCI DIO Card (RoHS). Includes one CA-4037W cable and two CA-4002 D-Sub connectors

Accessories:

- CA-3710: DB-37 Male-Male D-sub cable 1M (45º)
- CA-3710DM: DB-37 Male-Male D-sub cable 1M (180º)
- DN-37: DIN-Rail Mounting 37-pin Connector (Pitch=5.08mm)
- DN-37-381: DIN-Rail Mounting 37-pin Connector (Pitch=3.81mm)
- DB-37: Directly connect signal to D-Sub 37-pin connector

Attention!

If any of these items are missing or damaged, please contact your local field agent. Save the shipping materials and carton in case you want to ship or store the product in the future.

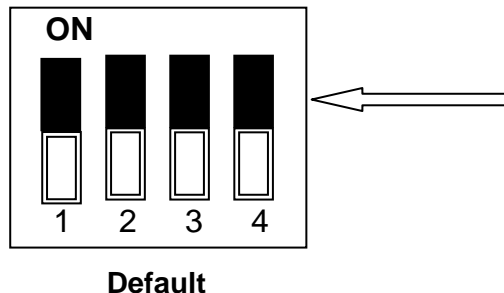# 2. Hardware Configuration

2.1. Board Layout
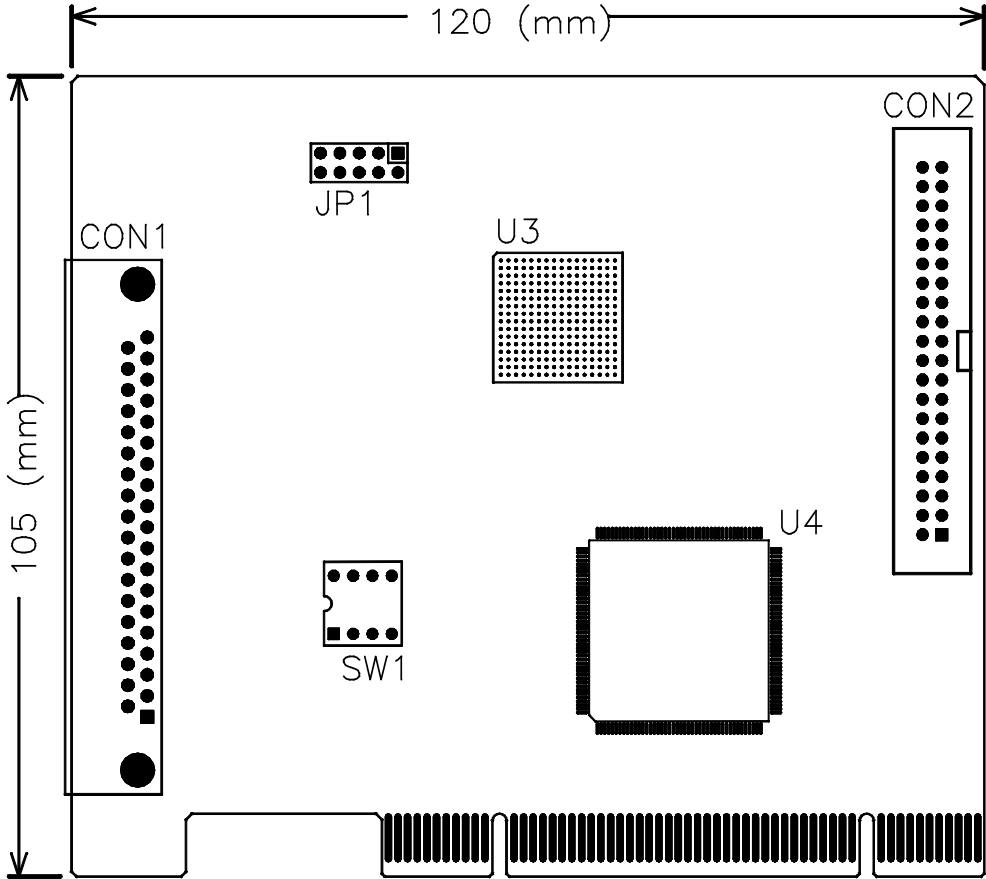
Item	Description
CON1	I/O connector (37-pin D-Sub female)
CON2	I/O connector (40-pin Box Header)
SW1	Card ID switch
JP1	Factory reserved

2.2. Card ID Switch Setting

SW1: Card ID Switch

The SW1 switch is used to set the card ID. The value is from 0 to 15. Please refer to table below for details.
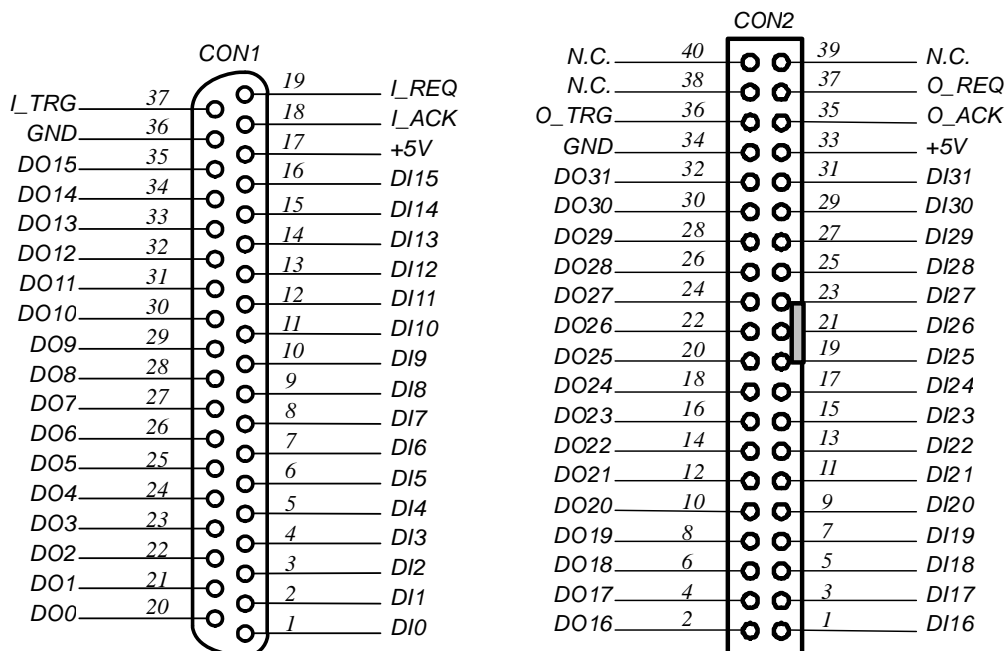
Card ID	Switch Setting (On = 1)			
	1	2	3	4
0(Default)	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

ON

1 2 3 4

Default

2.3. Pin Assignment

The PCI-D64HU has one 37-pin D-Sub connector (CON1) and one 40-pin pin header (CON2). Please refer figure below for the pin assignment of CON1 and CON2

Signal Name	Description	Direction
DIx	Digital input channel x	Input
DOx	Digital output channel x	Output
GND	Ground of all signals	Power
+5V	+5V power output (Max. 400 mA per pin)	Power
I_TRG	Trigger input to start DI sampling	Input
I_REQ	Request input for DI handshaking	Input
I_ACK	Acknowledge output for DI handshaking	Output
O_TRG	Trigger output controlled by software	Output
O_REQ	Request output for DO handshaking	Output
O_ACK	Acknowledge input for DO handshaking	Input

CON1

I_TRG	37	19	I_REQ
GND	36	18	I_ACK
DO15	35	17	+5V
DO14	34	16	DI15
DO13	33	15	DI14
DO12	32	14	DI13
DO11	31	13	DI12
DO10	30	12	DI11
DO9	29	11	DI10
DO8	28	10	DI9
DO7	27	9	DI8
DO6	26	8	DI7
DO5	25	7	DI6
DO4	24	6	DI5
DO3	23	5	DI4
DO2	22	4	DI3
DO1	21	3	DI2
DO0	20	2	DI1
		1	DI0

CON2

|			
N.C.	40	39	N.C.
N.C.	38	37	O_REQ
O_TRG	36	35	O_ACK
GND	34	33	+5V
DO31	32	31	DI31
DO30	30	29	DI30
DO29	28	27	DI29
DO28	26	25	DI28
DO27	24	23	DI27
DO26	22	21	DI26
DO25	20	19	DI25
DO24	18	17	DI24
DO23	16	15	DI23
DO22	14	13	DI22
DO21	12	11	DI21
DO20	10	9	DI20
DO19	8	7	DI19
DO18	6	5	DI18
DO17	4	3	DI17
DO16	2	1	DI16

2.4. Operation Theory

The PCI-D64HU support 4 data transfer modes, they are direct programmed I/O control, timer pacer control, external clock mode and handshaking mode. This chapter descript the detailed operation of these 4 data transfer modes.

Direct Program Control Mode

The status of digital inputs and digital outputs can be directly accessed by I/O port access. The I/O port address is assigned by system BIOS, please refer to the function reference manual for more detailed description.

Internal Timer Pacer Mode

There are three 16-bit timers on board. Timer#0 is for DI update and Timer#1 is for DO update. Both Timer#0 and Timer#1 can be optionally cascaded with Timer#2 for slower timer pacer generation. The base clock of all timers can be programmed from 20 MHz to 2.5 MHz (40 MHz / n; where n = 2 ~ 16).
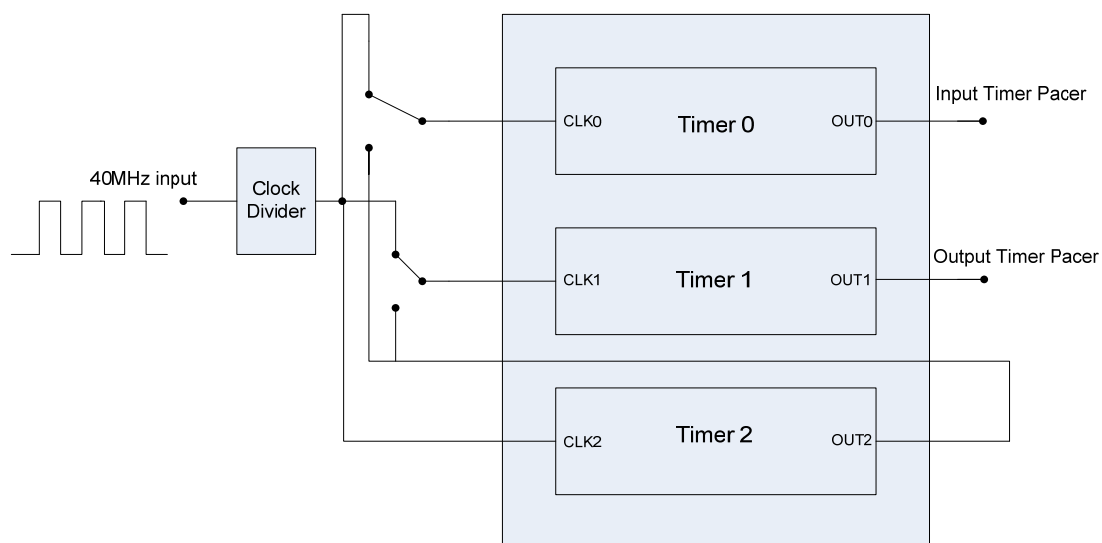
For digital input, the input data will be saved into DI FIFO after a timer pacer pulse is generated. When the DI FIFO is not empty, the saved data will be automatically transferred to the main memory of computer system by the bus mastering DMA controller.

For digital output, the state of output pins will be updated by the data in DO FIFO after a timer pacer pulse is generated. When the DO FIFO is not full, data in the main memory will be automatically transferred to the DO FIFO by the bus mastering DMA controller.

External Clock Mode (DI Only)

The digital input is clocked by external strobe, which is from Pin 19 (I_REQ) of CON1.

The input data will be saved into DI FIFO after a strobe is generated. When the DI FIFO is not empty, the saved data will be automatically transferred to the main memory of computer system by the bus mastering DMA controller.
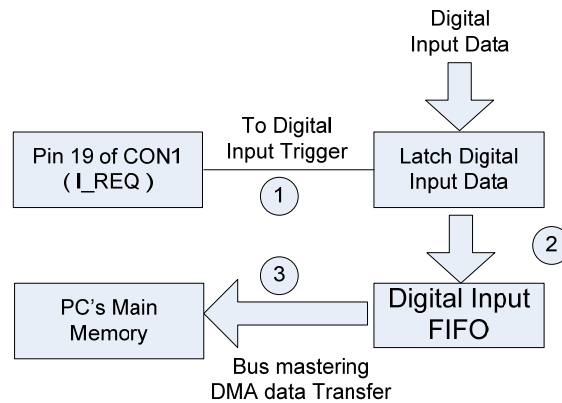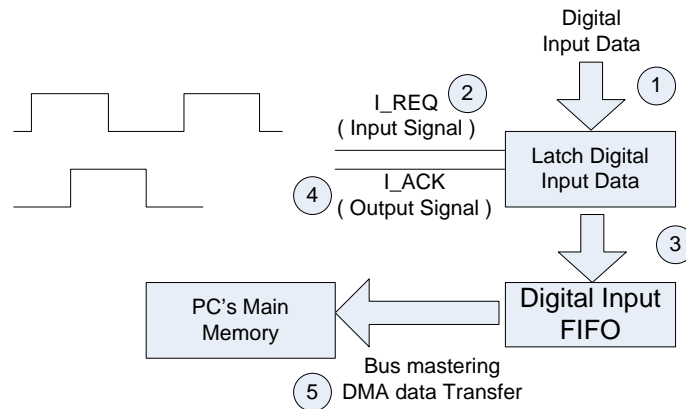

1. Digital Input data is ready and an I_REQ signal is generated by external device.
2. Digital input data is saved to FIFO.
3. If the FIFO is not empty and PCI bus is not occupied, the data will be transferred to main memory.

Handshaking Mode

The PCI-D64HU also supports handshaking data transfer mode. The data transfer rate is controlled by REQ and ACK signals to guarantee no data loss.

The operation of DI Handshaking

1. Digital Input data is ready.
2. An I_REQ signal is generated by external device.
3. Digital input data is saved to FIFO.
4. An I_ACK signal is generated and sent to the external device.
5. If the FIFO is not empty and PCI bus is not occupied, the data will be transferred to main memory.

The operation of DO Handshaking
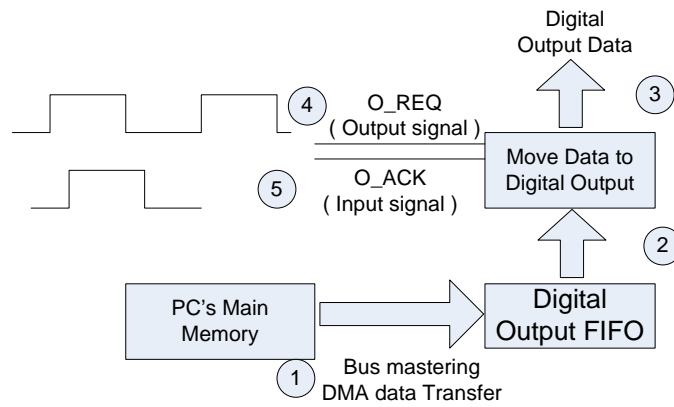
1. Digital output data is moved from PC's memory to DO FIFO by bus mastering DMA data transfer.

2. Move output data from FIFO to digital output circuit.

3. Output data is ready.

4. An O_REQ signal is generated and sent to the external device.

5. After an O_ACK is captured, steps 2-5 will be repeated.

** If the FIFO is not full, the output data is moved form PC's

main memory to FIFO automatically.

DO Ring Buffer Mode

The ring buffer is managed in hardware level and the size of the ring buffer can be set by user. When the DO FIFO is set as ring buffer mode, the last buffer of the DO buffer will be chained with the first buffer. No bus loading is required which makes PCI-D64HU perfect for repetitive pattern generation application.
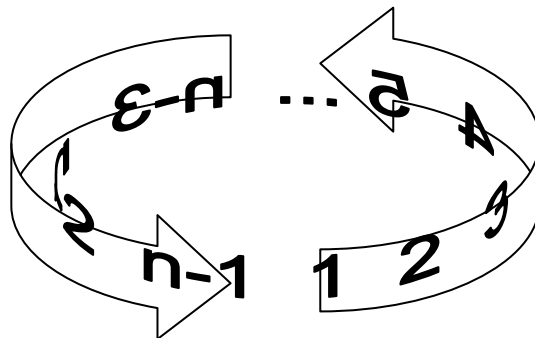
# 2.5. Timing Characteristic

Characteristic of Input Digital Filter

The digital filter is applicable for all DI signals, IREQ, ITRG and OACK. The maximum removable noise width can be programmed from (1~127) x 25ns.

System CLK 40MHz

I_REQ   tHOLD

tDelay

FLT_REQ   tLatch

DI0~DI31   Valid data
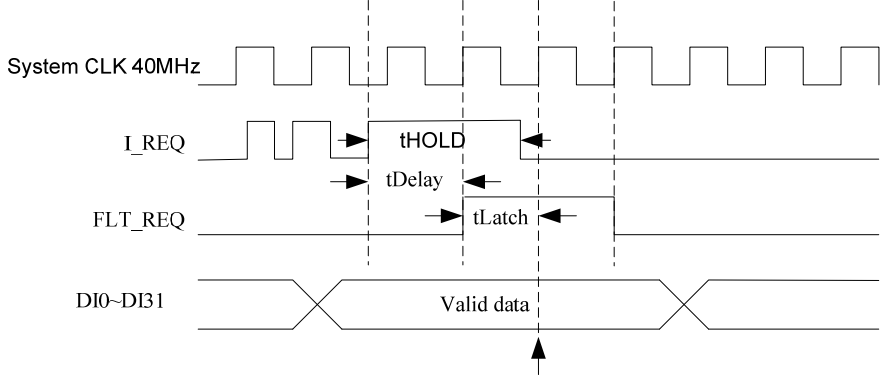
$n * 25ns < tDelay <= (n+1) * 25ns$	$tHold >= (n+1) * 25ns$	$tLatch = 25ns$

Where n=1~127

Characteristic of Output Pulse Extender in Timer Pacer Mode

System CLK 40MHz

O_REQ
(Output Signal)   tL

DO0 ~ DO31
(Output Signal)   Valid Data

tS   tH
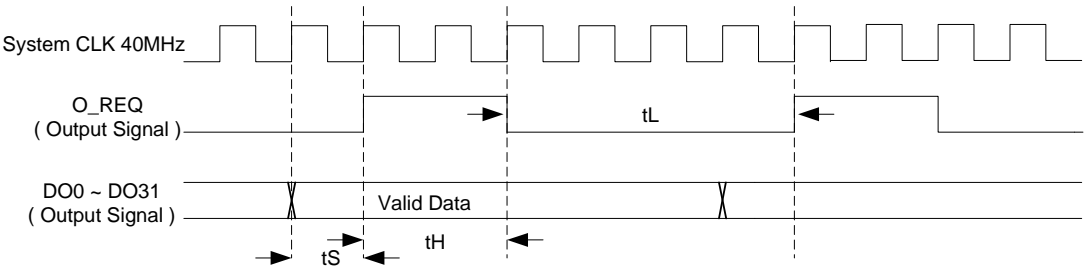
$25ns <= tS <= (2\wedge(n+1)) * 25ns$	$tH = (2\wedge(n+1)) * 25ns$
$tL >= (2\wedge(n+1)) * 25ns$	

Notes: n = 0~7

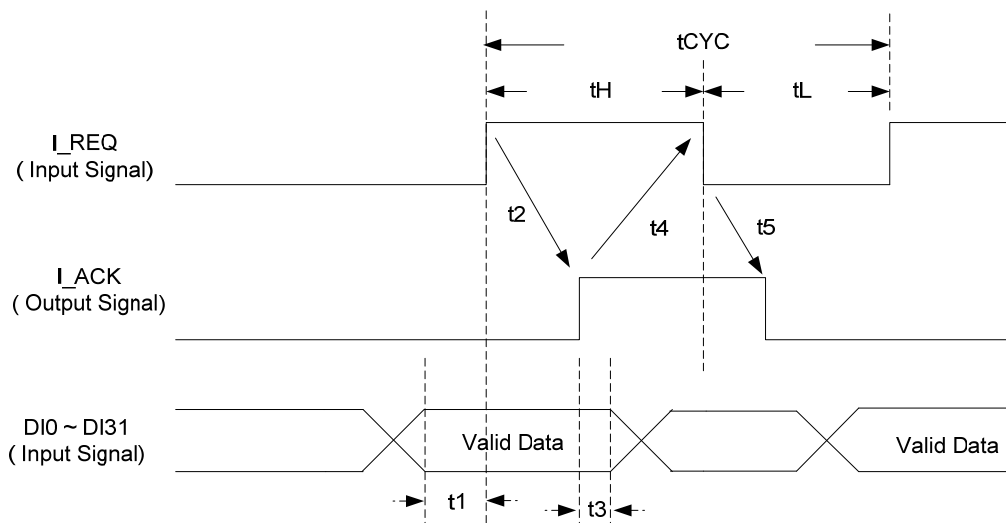## Characteristic of IREQ in External Clock Mode

IREQ Rising Edge Trigger:

I_REQ
(Input Signal)

tL

tH

tCYC

DI0 ~ DI31
(Input Signal)

Valid Data

tS
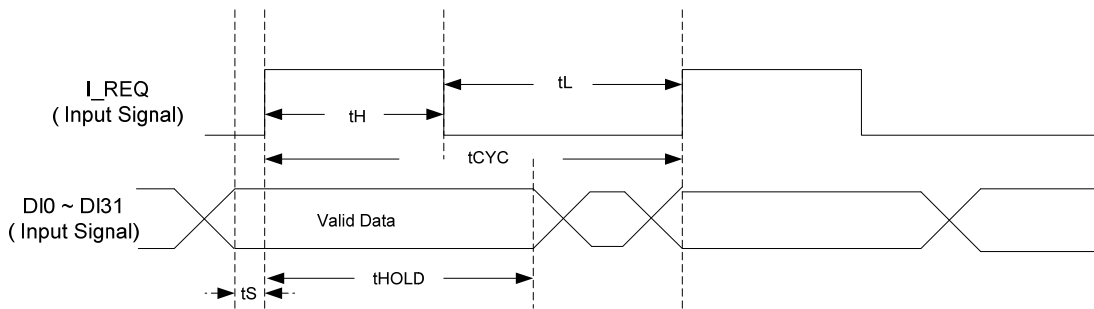
tHOLD

tH >= 25ns	tL >= 25ns	tCYC >= 100ns
tS >= 1ns	tHOLD >= 25ns	

IREQ Falling Edge Trigger:

I_REQ
(Input Signal)

tL

tH

tCYC

DI0 ~ DI31
(Input Signal)

Valid Data

tS
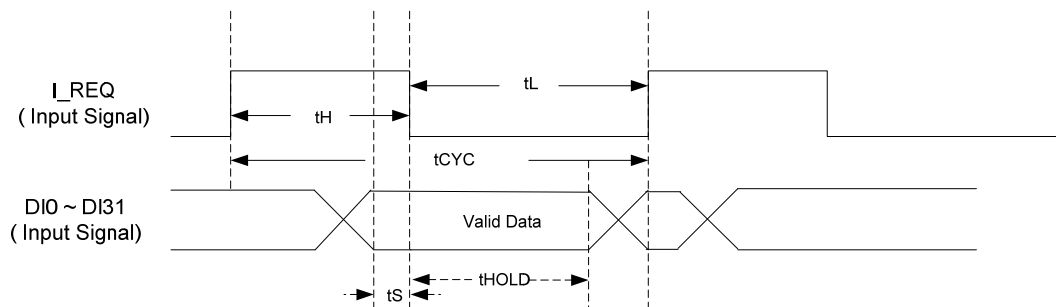
tHOLD

tH >= 25ns	tL >= 25ns	tCYC >= 100ns
tS >= 1ns	tHOLD >= 25ns	

Characteristic of DI Handshaking Mode

t1 >= 1ns	0ns < t2 < 29ns	t3 > 0ns	t4 > 0ns
0ns < t5 < 29ns	tH >= 25ns	tL >= 25ns	tCYC >= 100ns

Characteristic of DO Handshaking Mode
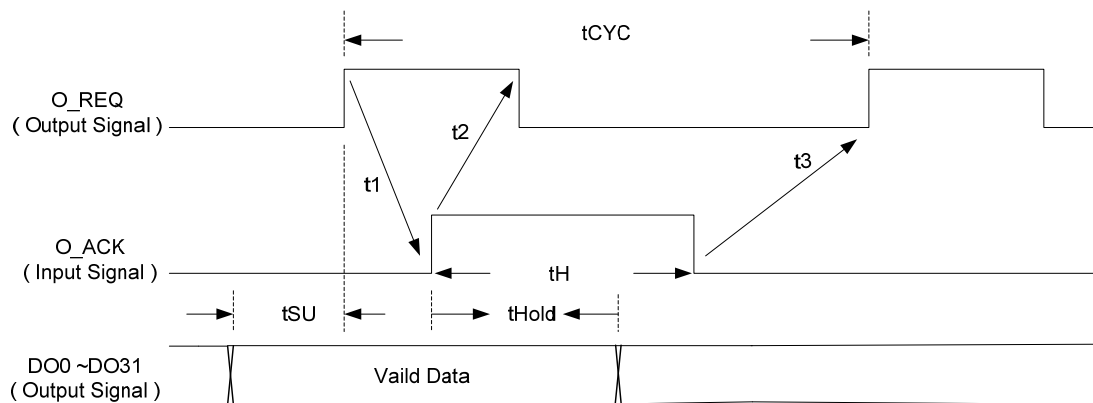
t1 > 0ns	0ns < t2 < 36ns	0ns< t3 < 36ns	tH >= 25ns
tSU = 25ns	25ns < tHold < 61ns	tCYC >= 100ns	