

# ISO-730

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## User's Manual

### **Warranty**

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# ISO-730

## 1. Introduction

The ISO-730 has 32 isolated digital I/O channels (16 D/I and 16 D/O) and 32 TTL digital I/O channels. Each of the 16 isolated digital input channels accept voltage from 5V to 24V and has 1.2 K $\Omega$  resistance of. Every eight input channels use one external common ground. For example, channel 0-7 use EI.COM1 and channel 8-15 use EI.COM2. Each of the 16 isolated digital output channels equipped a darlington transistor. Every eight output channels use the common emitter. The power supply of the output port should use the external power. The channels 0-7 uses EO.COM1 and channels 8-15 use EO.COM2. The board interface to field logic signals, eliminating ground-loop problems and isolating the host computer from damaging voltages.

The ISO-730 has one 37-pin D-Sub connector and four on-board 20-pin flat-cable connectors. It is fully compatible to PCL-730.

- 16 isolated digital input , 16 isolated open-collector output
- 16 non-isolated TTL inputs and 16 non-isolated TTL outputs.
- PC AT compatible ISA bus
- Interrupt level: 2,3,4,5,6,7 and jumper selectable.
- High current sink for isolated open-collector output( 200mA max.)
- 2500Vdc isolation on isolated I/O channels.
- D-sub connector for isolated I/O.

## Product Check List

In addition to this manual, the package includes the following items:

- ISO-730
- Demo program diskette

### **Attention!**

If any of these items is missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want ship or store the product in the future.

# 1.1 Specifications

## Digital Input

- 16 optically-isolated inputs  
Input voltage: 5 to 24Vdc  
Input resistance: 1.2K $\Omega$  / 0.5W  
Isolation voltage: 2,500V
- 16 TTL digital inputs (Non-isolation)  
Input voltage:  
Low : 0.8V (max.)  
High : 2.0V (min.)

## Digital Output

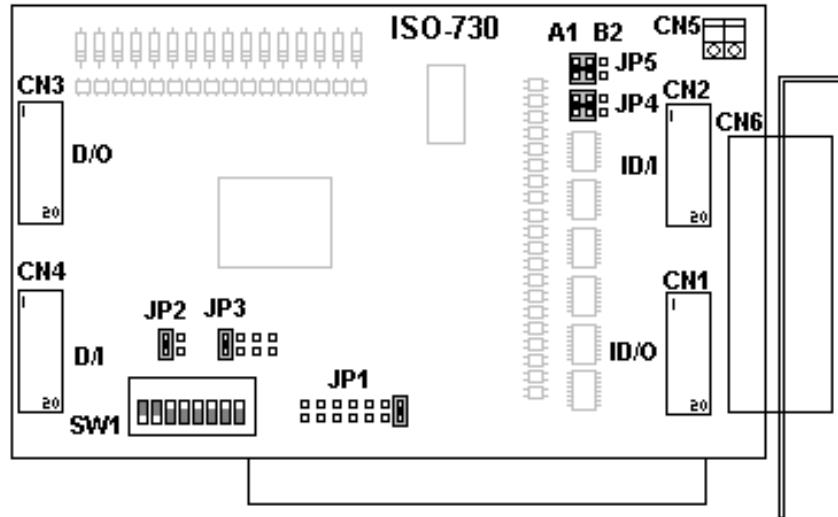
- 16 isolated open-collector output  
Per channel sink current: 200mA (max.)  
Output voltage: 5~40Vdc  
Isolation voltage: 2500Vdc
- 16 TTL-level outputs  
Output voltage: Low : Sink 8mA at 0.5Vmax.  
High : -0.4mA at 2.4V min.

## Interrupt Source

- Jumper selectable:
- Channels 0 and 1 of Isolated DI port
  - Channels 0 and 1 of TTL DI port

## 2. Hardware Configuration

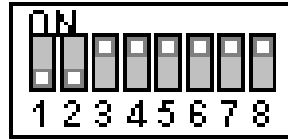
### 2.1 Board Layout



CN1	Isolated Open-collector Output
CN2	Isolated Digital Input
CN3	Digital Output
CN4	Digital Input
CN5	E.GND ( External Ground)
CN6	Isolated Input / Output
JP1	Interrupt Level
JP2	Interrupt Trigger
JP3	Interrupt Source
JP4,5	Version Control (A1,B2)
SW1	Base Address

## 2.2 I/O Base Address Setting

The ISO-730 occupies 4 consecutive I/O address space. The base address is set by DIP switch SW1. The default address is 0x300(hex).



A(  $\overline{9}$   $\overline{8}$   $\overline{7}$   $\overline{6}$   $\overline{5}$   $\overline{4}$   $\overline{3}$   $\overline{2}$  )

SW1: Base Address

Address	A9	A8	A7	A6	A5	A4	A3	A2
200h	OFF	ON	ON	ON	ON	ON	ON	ON
204h	OFF	ON	ON	ON	ON	ON	ON	OFF
208h	OFF	ON	ON	ON	ON	ON	OFF	ON
20Ch	OFF	ON	ON	ON	ON	ON	OFF	OFF
:	:	:	:	:	:	:	:	:
2F8h	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON
2FCh	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
*300h	OFF	OFF	ON	ON	ON	ON	ON	ON
304h	OFF	OFF	ON	ON	ON	ON	ON	OFF
308h	OFF	OFF	ON	ON	ON	ON	OFF	ON
30Ch	OFF	OFF	ON	ON	ON	ON	OFF	OFF
310h	OFF	OFF	ON	ON	ON	OFF	ON	ON
314h	OFF	OFF	ON	ON	ON	OFF	ON	OFF
:	:	:	:	:	:	:	:	::
330h	OFF	OFF	ON	ON	OFF	OFF	ON	ON
334h	OFF	OFF	ON	ON	OFF	OFF	ON	OFF
338h	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
33Ch	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
:	:	:	:	:	:	:	:	:

\*Default addresses setting

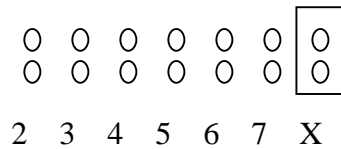
## 2.2.1 The I/O port mapping

I/O address	Device
0x000 ~ 0x1FF	PC reserved
0x200 ~ 0x20F	Game controller
0x278 ~ 0x27F	LPT2
0x2F8 ~ 0x2FF	COM2
0x300 ~ 0x31F	Prototype Card
0x320 ~ 0x32F	XT fixed disk
0x378 ~ 0x37F	LPT2
0x380 ~ 0x38F	SDLC
0x3A0 ~ 0x3AF	SDLE
0x3B0 ~ 0x3BF	Monochrome card
0x3C0 ~ 0x3CF	EGA card
0x3D0 ~ 0x3DF	CGA card
0x3F0 ~ 0xFF	Diskette controller , COM1

## 2.3 Jumper Setting

### 2.3.1 JP1 Interrupt Level

Using JP1 to select interrupt level from IRQ2 to IRQ7 , as shown below.

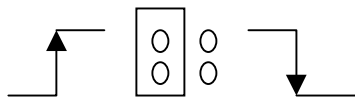


Default Setting

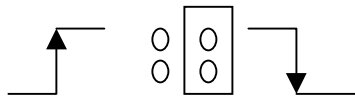
(X: Disable the interrupt)

### 2.3.2 JP2 Interrupt Trigger

Using JP2 to select the trigger edge on which the ISO-730 will trigger an interrupt.



Rising edge (Default)

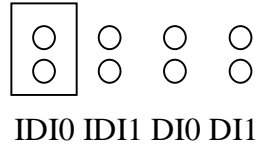


Falling edge



### 2.3.3 JP3 Interrupt Source

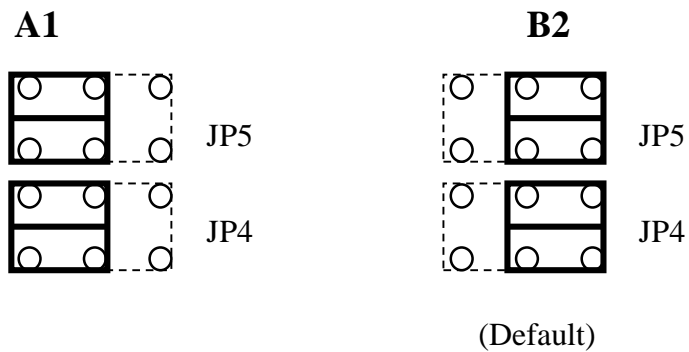
Using JP3 to select the source of the interrupt.



Select	D/I channel	Connector
IDI0	Isolated D/I channel 0	CN2 Pin 1 or CN6 Pin 1
IDI1	Isolated D/I channel 1	CN2 Pin 2 or CN6 Pin 20
DI0	TTL D/I channel 0	CN4 Pin 1
DI1	TTL D/I channel 1	CN4 PIN 2

### 2.3.4 JP4/JP5 Version selection

The JP4 and JP5 control the pin assignment of CN1,CN2 and CN6.  
Make sure your setting first.

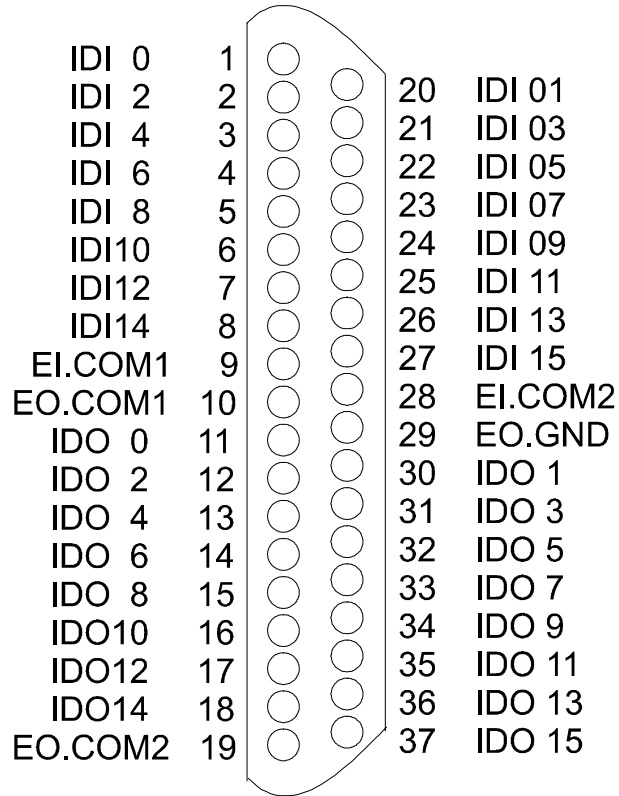


## 2.4 Pin Assignment

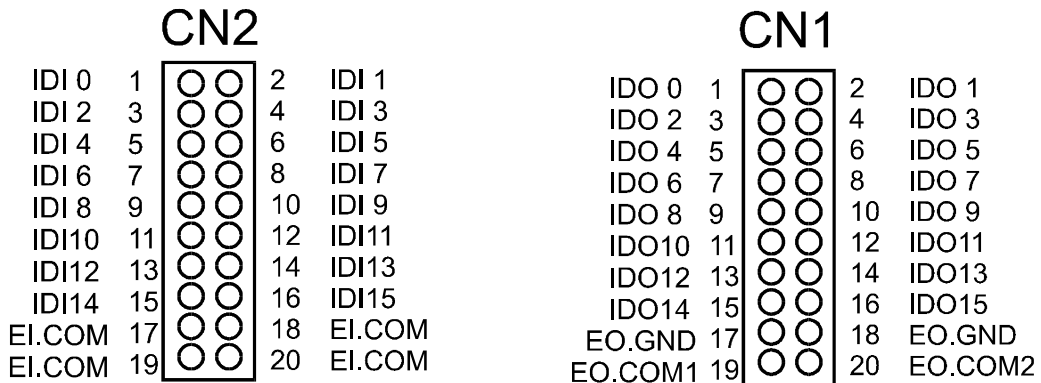
Before you use ISO-730 , please make sure JP5/ JP4 position is in A1 or B2.

### 2.4.1 Pin-Assignment of B2 Version

CN6: 37-pin D-sub connector



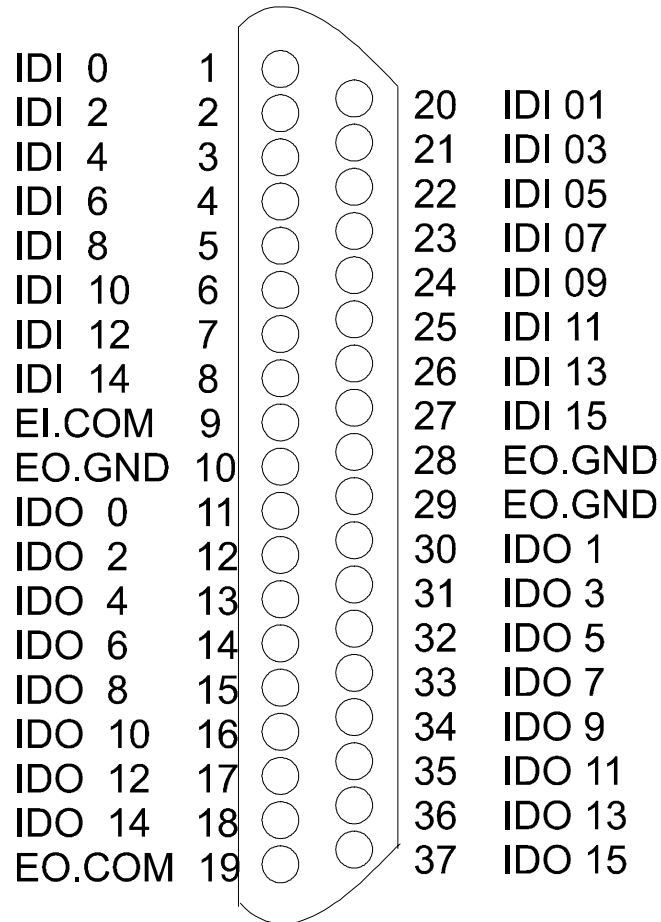
CN1 / CN2 Pin-Assignment



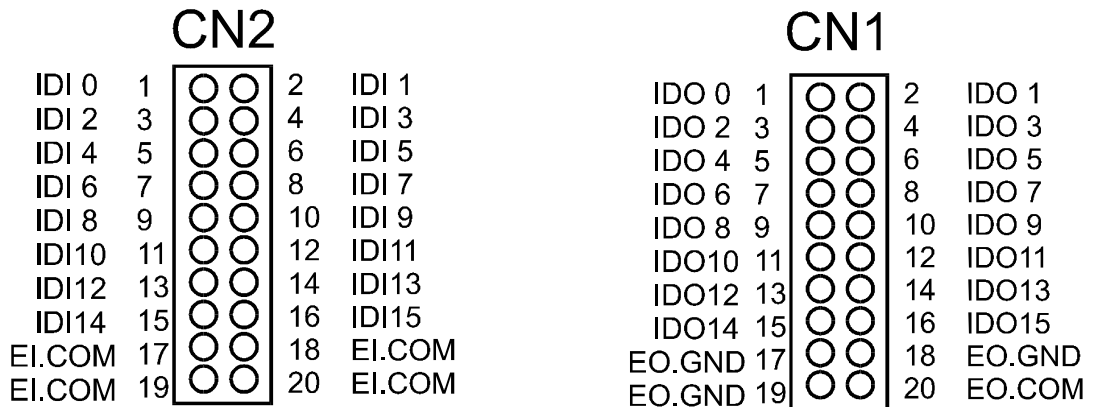
Isolated Digital input/output (B2)

## 2.4.2 Pin-Assignment of A1 Version

CN6 Pin-Assignment of A1 version



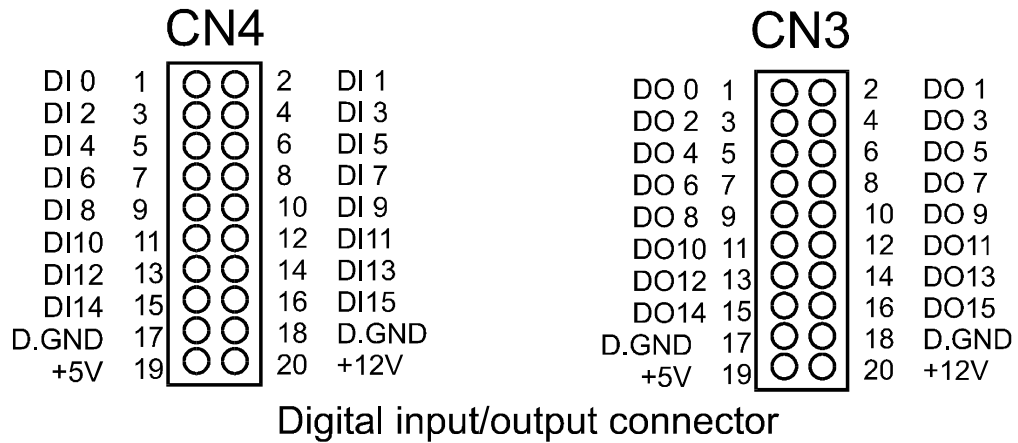
CN1 / CN6 Pin-Assignment of A1 Version



Isolated Digital input/output (A1)

## 2.4.5 TTL I/O Pin-Assignment of CN4 / CN3

The CN4 and CN3 are TTL-level digital input/ output ports. It can accept DB-16P and DB-16R series daughter board or other TTL-level signals.

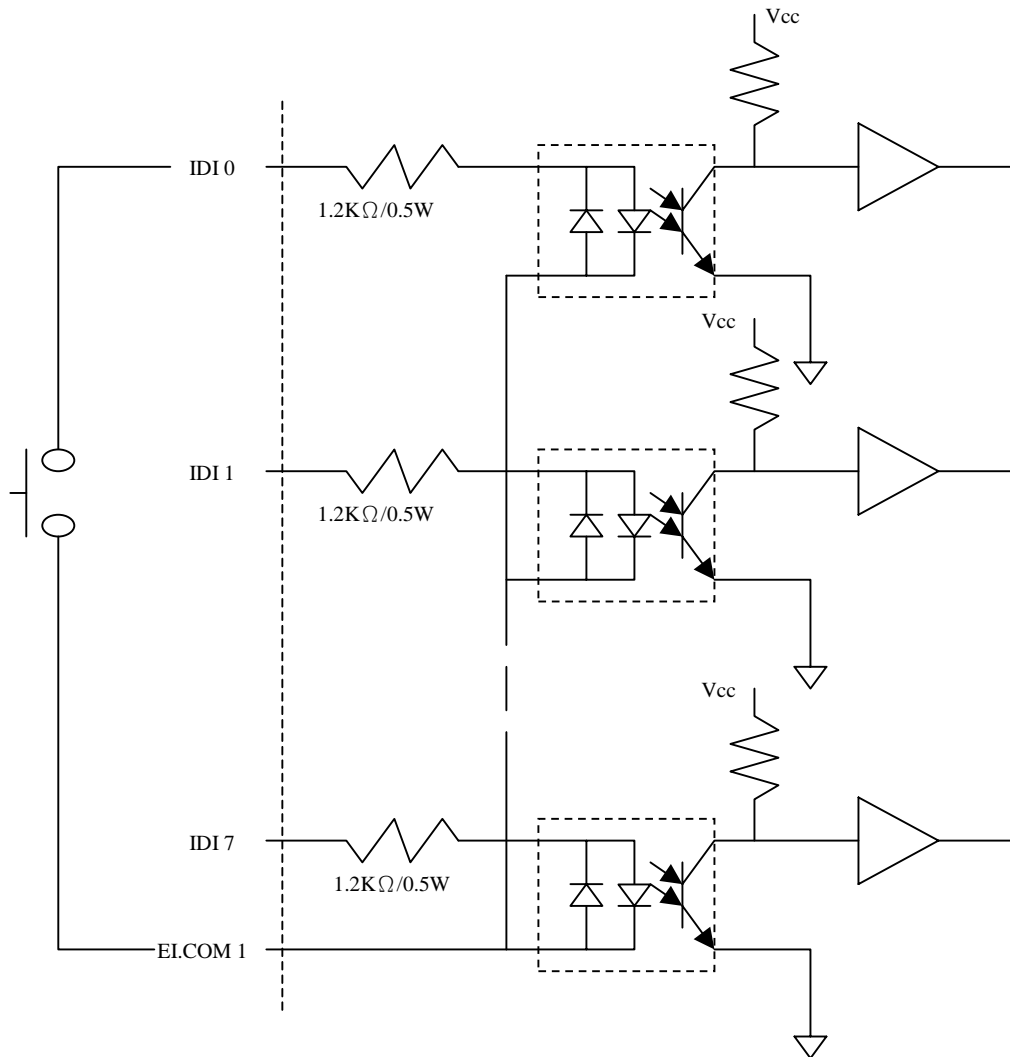


## 2.5 Digital I/O

### 2.5.1 Isolated Input (CN2 / CN6)

The ISO-730 provides 16 channel isolated digital inputs. Each of the 16 isolated digital input accept voltages from 5 to 24Vdc. Every eight input channels share one external ground.

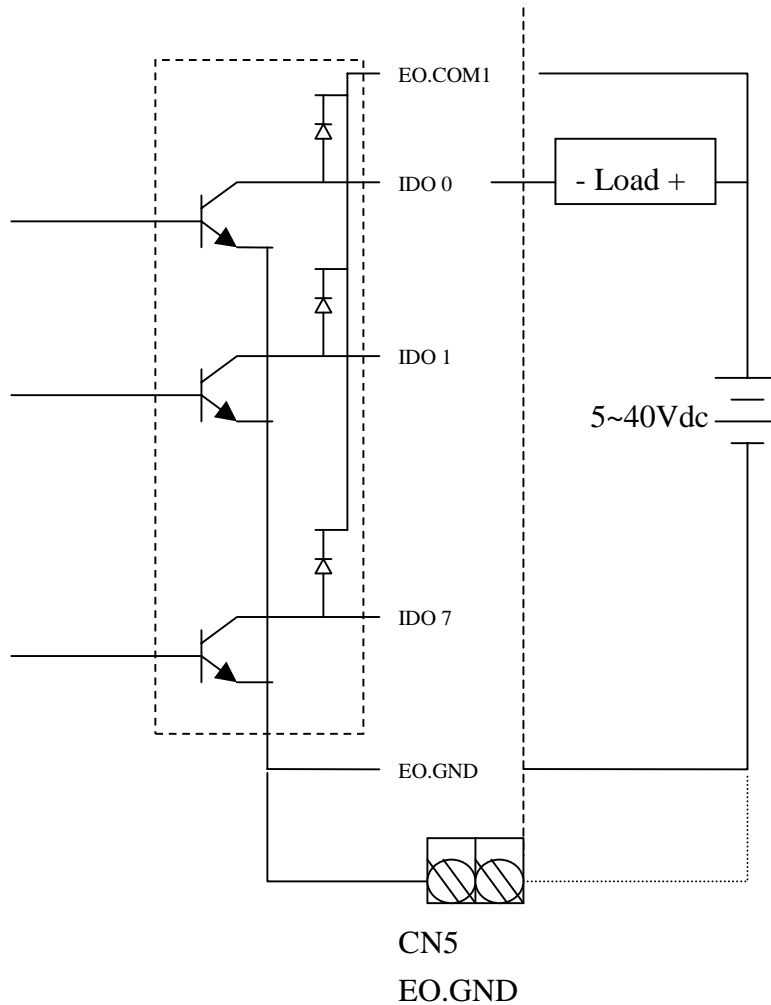
Channels 0-7 use EI.COM1, Channels 8~15 use EI.COM2 (B2 Version)



## 2.5.2 Isolated Open-collector Output

Every eight open-collector output channels share EO.COM. (Channel 0~7 use EO.COM1 , channel 8~15 use EO.COM2)

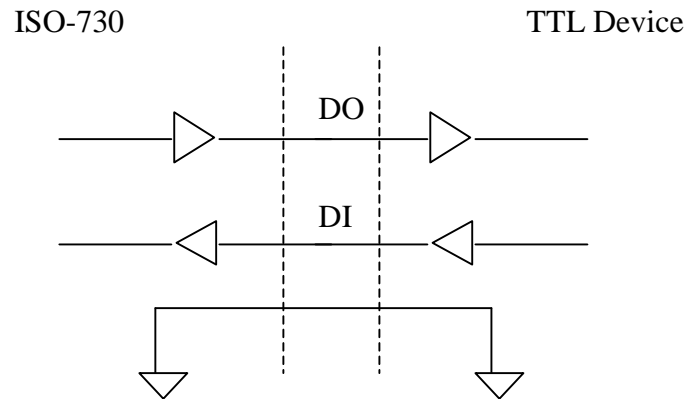
The maximum load of each channel is 5~40Vdc / 200mA. If the current of each channel exceeds 150mA, please use the connector CN5 to return the current to the external power .



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## 2.5.3 TTL Digital I/O

The ISO-730 provides 16 TTL level digital input channels and 16 TTL level digital output channels.



### 3. I/O Register Address

The ISO-730 card occupies 4 consecutive I/O addresses. The registers and their locations is shown in the following table.

ISO-730 Address Register

Address	Read	Write
Base+0	IDI Channel 0~7	IDO Channel 0~7
Base+1	IDI Channel 8~15	IDO Channel 8~15
Base+2	DI Channel 0~7	DO Channel 0~7
Base+3	DI Channel 8~15	DO Channel 8~15

IDI: Isolated Digital input

IDO: Isolated Open-collector output

DI: TTL Digital input

DO: TTL Digital output

The I/O channel of ISO-730 corresponds to a bit in the registers of the card. The channels and their register is shown in the following table.

Read/Write Base+0 (Isolated Digital I/O)

<b>Bit</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Channel</b>	7	6	5	4	3	2	1	0

Read/Write Base+1 (Isolated Digital I/O)

<b>Bit</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Channel</b>	15	14	13	12	11	10	9	8

Read/Write Base+2 (TTL Digital I/O)

<b>Bit</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Channel</b>	7	6	5	4	3	2	1	0

Read/Write Base+3 (TTL Digital I/O)

<b>Bit</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Channel</b>	15	14	13	12	11	10	9	8



## 3.1 Programming

### For C Language:

```

Main()
{
int Io_add = 0x300;          /* 730 I/O Address = 0x200 Default setting */
int In_p0,In_p1, In_p2,In_p3;

outputb( Io_add+0 , 0xaa ); /* output data '1010 1010' to con2 ID/O Channel 0~7 */
outputb( Io_add+1 , 0x55); /* output data '0101 0101' to con2 ID/O channel 8~15 */
outputb( Io_add+2 , 0xaa ); /* output data '1010 1010' to con1 D/O Channel 0~7*/
outputb( Io_add+3 , 0x55); /* output data '0101 0101' to con1 D/O Channel 8~15 */

In_p0=Inportb(Io_add+0);   /* Read CON 2 ID/I Channel 0~7 Data */
In_p1=Inportb(Io_add+1);   /* Read CON 2 ID/I Channel 8~15 Data */
In_p2=Inportb(Io_add+2);   /* Read CON 1 D/I Channel 0~7 Data */
In_p3=Inportb(Io_add+3);   /* Read CON 1 D/I Channel 8~15 Data */
}

```

### For Quick Basic Language

```

Bas=&h300
OUT Bas+0, &HAA    ' output data '1010 1010' to CON 2 ID/O Channel 0~7
OUT Bas+1, &H55    ' output data '0101 0101' to CON 2 ID/O Channel 8~15

OUT Bas+2, &HAA    ' output data '1010 1010' to CON 1 D/O Channel 0~7
OUT Bas+3, &H55    ' output data '0101 0101' to CON 1 D/O Channel 8~15

P0=inp(Bas+0)      ' Read CON 2 ID/I Channel 0~7 data
P1=inp(Bas+1)      ' Read CON 2 ID/I Channel 8~15 data
P2=inp(Bas+2)      ' Read CON 1 D/I Channel 0~7 data
P3=inp(Bas+3)      ' Read CON 1 D/I Channel 8~15 data

```